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FOREWORD

The proceedings contained herein are compiled and published by the Engineering Department, Naval Weapons Center, as supporting documentation for the 10th Annual Soldering/Manufacturing Seminar to be held on 19 and 20 February 1986 at NWC, China Lake, CA. This document is a compilation of information—some of it preliminary—that was provided by both nongovernment and government sources.

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(U) Presented are the proceedings of the 10th Annual Soldering/Manufacturing Seminar, held on 19 and 20 February 1986 at the Naval Weapons Center, China Lake, CA. The proceedings include the papers or abstracts of papers presented at the Seminar and cover all aspects of soldering technology and electronics manufacturing. The proceedings are a compilation of information–some of it preliminary–provided by both nongovernment and government sources. The proceedings are published in the interest of furthering communication and broadening awareness of current activities among soldering technology and electronics manufacturing specialists.

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Soldering technology training program
Solder joint failure
Solder properties
Statistical process control
Surface mounted devices
Wave soldering
Wetting balance

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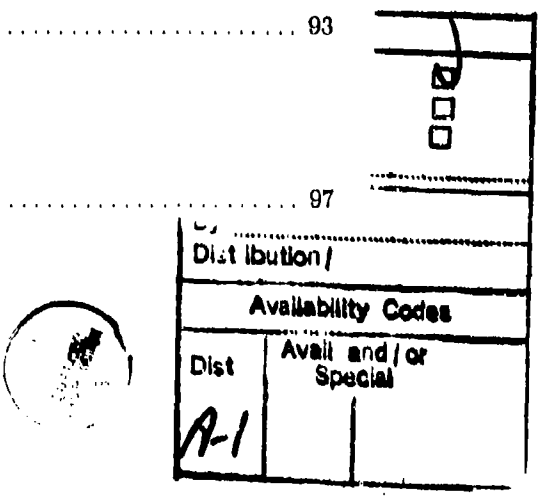

INTRODUCTION

The ever-changing, fast-paced technological advances being made today in soldering and electronics manufacturing present a challenge to us all. To help meet this challenge, we must work together. This Seminar—the 10th Annual Soldering/Manufacturing Seminar—gives us an excellent opportunity to do just that. This Seminar promotes an open exchange of information on all issues of soldering technology and electronics manufacturing. It provides a forum for all persons involved in this technology, whether from government, industry, or academia. Here we can openly discuss these issues and share our ideas. Here we can work together toward our common goal: to improve the U.S. electronics industrial base.

To help make this improvement we must work toward the goals of producibility and quality. We must maintain a concerted effort to resolve production-line problems. First, we must work to understand these problems. Then, we must develop process controls and methods to solve them. Because producibility and quality are inseparable, it is critical that our designers learn from past problems and that they design for ease of manufacturing. The Navy, through efforts at the Naval Weapons Center, is continuing to work with industry in the Soldering Technology Branch and in the Electronics Manufacturing Program Office.

The Soldering Technology Branch is continually working to ensure that we meet the goals of producibility and quality. We evaluate soldering requirements and provide these evaluations to government and industry facilities. The Navy's work to consolidate its soldering requirements has resulted in WS-6536E. We are continuing to work with DOD-STD-2000 and expect a Navy transition to that specification by mid-1987.

Another approach we are taking to improve our electronics industrial base is coordinated by the Electronics Manufacturing Productivity Facility (EMPF). The EMPF was established at the Naval Weapons Center in 1984. We are chartered, through the Office of Naval Acquisition Support (ONAS), to lead a cooperative effort between electronic equipment manufacturers, product manufacturers, and government agencies to test, evaluate, and research electronics manufacturing processes and materials. The EMPF coordinates the cooperative work of these groups to develop high-quality processes and to demonstrate high-quality manufacturing disciplines in a production environment. The EMPF documents this cooperative work and develops an accessible information source for electronics manufacturing productivity. Our goal is to gain information, share information, and use information to help produce high quality products at lower cost in less time.

We are indeed looking forward to working with you to improve our electronics industrial base.

Thank you for your interest in soldering technology and electronics manufacturing and for joining us at this Seminar.

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ARTIFICIAL AGING AND COMPONENT SOLDERABILITY

BY

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INTRODUCTION

The NWC Conference has long been one of the most powerful forums on soldering and solderability in the country. Participants have concentrated heavily on the solderability of component leads, and have had a great effect on how solderability is perceived and measured. As a result, numerous specifications have been tightened to ensure good solderability.

Our efforts have resulted in an overall industry awareness of solderability issues that is higher than ever before. But in order to help make further gains in lead solderability we will need to do more than just demand ever tighter specifications. To date, our view of soldering and solderability has been restricted to the component lead, with a goal of making the lead itself more solderable. We will need to take a broader view. For the lead is a system of materials that is part of a larger system of materials making up the component itself. The component is, in turn, part of a larger group of components that comprise the end-product.

As such, the lead will be subjected to two completely different manufacturing cycles: assembly into the component, followed by a period of storage, and then assembly into the end-product. All manufacturing steps, up to the final flow soldering into the printed wiring assembly (PWA), will have an effect on the solderability of the lead. Two good examples are axially leaded components and integrated circuits.

Axially leaded components can have leads that contain radically different plating systems. Tin, tin-lead, or gold can be plated over nickel, copper, or Kovar. Some may contain underplating or a barrier plate while others do not. After storage for an undetermined period of time, the lead is cut, formed, and assembled onto a component body. A housing or coating, such as epoxy, may be applied, followed by a curing bake. The finished part may then be subjected to a stabilizing bake, or one or more burn-in cycles. After another undetermined storage period, it is shipped to the end-user.

Integrated circuits follow a similar manufacturing path. The lead material typically consists of tin or tin-lead over Kovar or Alloy 42. Again after manufacture, the lead frame material is stored for an unknown period of time. When assembled into a part, it is bonded to a layer of ceramic. Once the silicon chip is installed, the lead frame is coated with glass frit and another layer of ceramic and fired. Any oxides resulting from the furnace bake are removed with an acid bath. Finally, the last two steps involve reflow of the electroplate or hot solder dip, and the burn-in cycle. The reflow step may be before or after burn-in. This is then followed by storage in the manufacturer's warehouse.

All of these parts are then shipped to the end-user where they are stored. Since many companies have a first in, random out warehouse, the parts could be stored for months or years before being used in production. After assembly, the PWA may be baked for 6 to 24 hours at 105 C to help remove moisture from the printed wiring board, preventing delamination during flow soldering. Finally, the PWA is preheated and flow soldered.

From this description it is obvious that any effective incoming solderability screen by the end-user on purchased parts must not only gauge the state of the plating system following part manufacture, but must also predict the effects of storage and assembly into the PWA. The test contained in MIL-STD-202F, Method 208E is intended to provide the needed solderability screen. A steam aging step for one hour is included in this test to simulate accelerated aging. Recently, questions concerning the validity of the one hour aging step have arisen. Proposals have been made to increase the time to 8 or even 24 hours. (Ref. 1, 2, 3)

This conference has worked hard and has generated a powerful force to make solderability testing what it wants it to be. We might be preparing to be too demanding. We cannot demand what is unattainable, but must first determine what is needed. When the changes do occur, both component manufacturers and users must be prepared in advance. Otherwise, the price will be extensive yield losses and rework.

In order to evaluate the effects of varying amounts of steam aging on part solderability, a representative cross-section of many different types of components contained in the warehouse at TI were chosen. The samples were then subjected to 1, 8, and 16 hours of steam aging, and the solderability test performed. The results of this testing are presented in Section I of this paper.

As a separate effort, Section II takes a more theoretical look at the activation energy for intermetallic growth and oxidation of the Sn-Pb/Cu system. This section correlates storage time and steam aging.

Finally, Section III gives a brief description of TI's efforts to improve the solderability of stranded wire purchased by the company.

I. AGING STUDY RESULTS

A study was undertaken to determine how the results of MIL-STD-202F, Method 208E solderability testing would be impacted by steam aging times of 1, 8, and 16 hours. The samples for the study form a representative cross-section of the most common components used in TI systems and available in the warehouse. The sample matrix encompasses a variety of device types, plating systems, and manufacturers. In total, 85 lots were included in the study. The method of packaging during warehouse storage was not considered. Five samples per lot were tested at each of the three aging intervals.

Samples from each of the 85 lots were microsectioned in the as-received condition to determine the base metal and the plating system, as well as the plating thickness. Solderability testing was accomplished using a steam ager built to the MIL-STD-202F, Method 208E guidelines, an Electrovert Model WDC flowing solder pot, and an HMP Model 1900 mechanical dipper. Both passing and failing parts were microsectioned following the test. The complete solderability test results are included in the Appendix to this report.

The following tables will summarize the test results. Six general plating schemes, twelve device types, five date codes, and twenty- four manufacturers were encompassed in this study. Table I summarizes the various plating schemes tested, and Table II summarizes the various device types tested.

Table I: Plating Systems

	# Lots
Tin or Tin-Lead over Nickel, Kovar, or Alloy 42	11
Gold over Nickel, Kovar, or Alloy 42	3
Tin or Tin-Lead over Kovar or Alloy 42 (All DIP ICs)	32
Tin or Tin-Lead over Copper over Nickel over Kovar or Alloy 42	3
Tin or Tin-Lead over Copper or Copper-Clad-Steel (CCS)	27
Gold over Nickel over CCS, Kovar or Alloy 42	9

Table II: Device Types

	# Lots		# Lots
Tantalum Capacitor	4	DIP IC	32
Polycarbonate Capacitor	3	IC (TO-39, TO-99)	9
Ceramic Capacitor	2	IC (TO-3)	3
Mica Capacitor	2	Transistor (TO-5)	2
Resistor	15	Transistor	2
Variable Resistor	3	Diode	8

Table III summarizes the overall solderability test results. On a part basis, only 67% passed the existing MIL-STD-202F, Method 208E solderability test. On a lot basis, that number falls to 48%. The number of lots that could actually be used would be improved by tinning the components utilizing fluxes more active than those used in testing. However, routine tinning is not an attractive alternative.

The test results appear to be date code independent since both sample quantities and test failures were equally distributed between parts with 1984 and 1985 date codes. This was expected since leads and lead frames are not assigned a date code and may be stored indefinitely before assembly into a component. Hence the date code as a purchasing parameter relating to solderability may never be of value because of the lack of correlation between component date codes and the date of lead manufacture. It must be re-emphasized, most of these parts have been in storage for 6 months to 1 1/2 years, and some even longer.

Table III: Solderability Results By Lead Types

Lead Type	# of Lots Tested	Percent Parts Passing			Percent Lots Passing		
		1 Hr	8 Hr	16 Hr	1 Hr	8 Hr	16 Hr
Sn or Sn/Pb over Kovar or Alloy 42	32	55	23	18	41	13	3
Sn or Sn/Pb over Cu or Cu-Clad-Steel	27	81	56	40	56	29	15
Au over Ni over Cu-Clad-Steel, Kovar or Alloy 42	9	96	91	73	78	66	45
Sn or Sn/Pb over Ni, Kovar, or Alloy 42	11	45	27	33	36	18	18
Sn or Sn/Pb over Cu over Ni over Kovar or Alloy 42	3	60	13	0	33	0	0
Au over Ni, Kovar, or Alloy 42	3	60	27	7	33	0	0
Overall Average	85	67	41	32	48	24	13

Tables IV through IX show detailed test results for each plating system. The largest group of samples was DIP ICs, shown in Table IV, having tin or tin-lead coated Kovar or Alloy 42 leads. The results show that 55% passed after one hour of steam aging. The occurrence of failures appeared to be independent of manufacturer, but did depend greatly on lead treatment. Electroplated and solder dipped leads were much more resistant to steam aging than were reflowed leads. Many of the failures were due to edge dewet in varying degrees. This can be expected since plating thickness is less near the edges, especially on reflowed parts.

Parts having leads consisting of tin or tin-lead over copper which includes axially leaded capacitors, resistors, and diodes performed relatively well at one hour. Table V shows that 81% of these parts passed. It is worth mentioning that lot numbers 25 and 26, of which none passed, were wirewound resistors with stamped leads. Typically, these have performed poorly in our solderability tests because the lead forming process uses pre-plated leads. Other failures were attributed to thick, brittle Cu-Sn intermetallics and to Cu-Sn intermetallics forming on parts with thin plating; the latter mechanism consuming all of the free tin. A similar problem arises in platings with high lead contents (70% - 90% wt). Even leads with 400 microinches of plating become unsolderable because of tin depletion after 100 microinches of intermetallic formation.

Data for the parts having the best overall solderability appear in Table VI, where it is shown that 96% of the parts having gold over nickel passed the Mil-Std solderability test. This is particularly interesting when one notes that the gold thicknesses are between 12 and 90 microinches. In contrast to this is the data in Table VII. Whereas the ICs in TO- packages performed well with a gold overplate, they performed poorly with a tin or tin-lead overplate. Unfortunately, no determination could be made as to whether this was due to the base metal preparation or to the overplate itself.

Looking back at Table III it can be seen that 41% of the parts passed after 8 hours of steam aging. As the components are presently made, only two plating systems held up reasonably well after extended aging. Superior was the gold over nickel system where 91% of the parts passed. Next was the tin or tin-lead over copper system with 56% of the parts passing. All of the other platings fared badly. The 16 hour aging time results show a further reduction in the percentage of passing parts to 32%, with the gold over nickel and tin or tin-lead over copper plating systems again performing best.

Figures 1 through 14 show photographs of representative test samples. They consist of parts which exhibited acceptable solderability at each steam aging, as well as parts that failed at each steam aging. Cross-sections of each part are also included. Figures 15 and 16 show cross-sections illustrating the various conditions in which leads have been received at TI. Each of these parts had solderability problems either at Incoming or on the assembly line. Figure 17 shows a cross-section of a capacitor lead. These parts exhibited dewetting on the assembly line. Attempts were made to tin the component lead so that they could be used. Figure 18 shows another part from the same lot which has been tinned. Note the Cu_3Sn intermetallic compound has been completely removed. The tinned parts were then solderability tested after extended steam agings. In no cases did failures occur. This indicates that the effects of component manufacturing on the leads can be corrected in some cases.

In summary, these test results indicate that the one hour of steam aging does not adequately insure shelf lives beyond 6 months. A longer steam aging step should be included to insure not only adequate shelf life, but also to insure the parts will be able to withstand the PWA manufacturing cycle. The only reason these parts do not present a greater problem during assembly is that the solder processes have been so finely tuned that compensations have been made for many of these problems. Any further increase in the producibility of these assemblies must involve an increase in lead solderability rather than simply more improvements in soldering techniques. Improvements in lead solderability must account for the effects of all manufacturing steps, both for the component itself and the PWA. The solderability of the plating system can thereby be optimized, and any deleterious effects compensated for or corrected.

TABLE IV: SOLDERABILITY RESULTS - SN OR SN/PB OVER KOVAR OR ALLOY 42 (DIPs)

ID	PART TYPE	SN OR SN/PB TREATMENT	DC	SOLDERABILITY TESTING NUMBER PASSED/5 TESTED 1 HR.	8 HR.	16 HR.
30	DIP IC	EP	8437	0	0	0
31	DIP IC	SD	8511	5	3	2
32	DIP IC	R	8448	0	1	0
34	DIP IC	R	8505	2	0	0
35	DIP IC	SD	8438	4	5	4
36	DIP IC	SD	8519	1	0	0
37	DIP IC	EP	8232	1	2	1
38	DIP IC	EP	8311	0	0	0
39	DIP IC	EP	8446	2	3	4
40	DIP IC	R	8423	0	0	0
41	DIP IC	EP	8442	5	3	4
42	DIP IC	SD	8412	2	0	0
43	DIP IC	SD	8516	5	0	0
44	DIP IC	EP	8416	0	0	0
45	DIP IC	R	8442	1	0	0
46	DIP IC	R	8522	0	0	0
47	DIP IC	EP	8436	5	0	2
48	DIP IC	EP	8502	5	5	5
49	DIP IC	EP	8429	5	2	0
50	DIP IC	EP	8303	4	0	0
51	DIP IC	SD	8505	5	0	0
52	DIP IC	EP	8430	3	1	1
54	DIP IC	SD	8520	2	0	0
55	DIP IC	EP	8537	5	5	4
56	DIP IC	R	8503	0	0	0
59	DIP IC	EP	????	5	2	1
80	DIP IC	R	8425	5	0	0
81	DIP IC	R	8504	1	0	0
82	DIP IC	SD	8427	5	0	0
83	DIP IC	SD	8534	5	5	0
84	DIP IC	EP	8509	5	0	1
85	DIP IC	R	8431	0	0	0
			OVERALL TOTAL	88	37	29
			% PASSING	55	23	18
			ELECTROPLATED (EP) TOTAL	45	23	23
			% PASSING	64	32	32
			REFLOWED ELECTROPLATE (R) TOTAL	9	0	0
			% PASSING	20	0	0
			HOT SOLDER DIPPED (SD) TOTAL	34	13	6
			% PASSING	76	32	15

TABLE V: SOLDERABILITY RESULTS - SN OR SN/PB OVER CU OR CU-CLAD-STEEL

ID	PART TYPE	DC	SOLDERABILITY TESTING NUMBER PASSED/5 TESTED 1 HR.	8 HR.	16 HR.
3	POLYCARB CAPACITOR	8438	4	2	2
4	POLYCARB CAPACITOR	8434	5	4	5
5	POLYCARB CAPACITOR	8438	3	2	1
8	CERAMIC CAPACITOR	8545	5	3	0
9	CERAMIC CAPACITOR	8518	4	0	1
14	MICA CAPACITOR	8523	5	3	0
15	MICA CAPACITOR	8542	5	2	5
6	RESISTOR	8449	5	4	2
7	RESISTOR	8505	5	4	4
10	RESISTOR	8530	5	5	0
11	RESISTOR	8325	5	5	5
12	RESISTOR	8401	5	3	0
13	RESISTOR	8343	3	3	0
18	RESISTOR	????	0	0	1
19	RESISTOR	8414	4	5	2
23	RESISTOR	8503	5	0	5
24	RESISTOR	8443	5	2	3
25	RESISTOR	8446	0	0	0
26	RESISTOR	8327	0	0	0
28	RESISTOR	8416	5	0	2
29	RESISTOR	8439	4	0	0
69	DIODE	8520	5	4	4
70	DIODE	8444	5	5	4
72	DIODE	8516	5	5	3
73	DIODE	????	4	5	0
74	DIODE	8525	4	5	4
75	DIODE	8407	4	5	1
		TOTAL	109	76	54
		% PASSING	81	56	40

TABLE VI: SOLDERABILITY RESULTS - AU OVER NI OVER CCS, KOVAR, OR ALLOY 42

ID	PART TYPE	DC	SOLDERABILITY TESTING NUMBER PASSED/5 TESTED 1 HR.	8 HR.	16 HR.
58	IC (TO-99)	8424	5	4	4
60	IC (TO-39)	8525	5	5	5
61	IC (TO-99)	8342	5	5	5
63	IC (TO-99)	8530	5	3	2
65	IC (TO-39)	8435	4	5	3
67	IC (TO-99)	8510	5	5	5
71	TRANSISTOR	8428	5	4	1
76	DIODE	8441	5	5	5
77	DIODE	8525	4	5	3
		TOTAL	43	41	33
		% PASSING	96	91	73

TABLE VII: SOLDERABILITY RESULTS - SN OR SN/PB OVER NI, KOVAR, OR ALLOY 42

ID	PART TYPE	DC	SOLDERABILITY TESTING NUMBER PASSED/5 TESTED 1 HR.	8 HR.	16 HR.
1	TANTALUM CAPACITOR	8320	5	5	4
2	TANTALUM CAPACITOR	8250	4	2	2
16	TANTALUM CAPACITOR	8516	5	1	5
17	TANTALUM CAPACITOR	8541	5	2	2
22	RESISTOR	8348	5	5	5
27	VAR. RESISTOR	8109	0	0	0
33	IC (TO-3)	8216	0	0	0
57	IC (TO-99)	8009	0	0	0
62	IC (TO-3)	8505	0	0	0
66	IC (TO-99)	8315	1	0	0
68	TRANSISTOR	8509	0	0	0
		TOTAL	25	15	18
		% PASSING	45	27	33

TABLE VIII: SOLDERABILITY RESULTS - SN OR SN/PB OVER CU OVER NI OVER KOVAR OR ALLOY 42

ID	PART TYPE	DC	SOLDERABILITY NUMBER PASSED/5 TESTED 1 HR.	8 HR.	16 HR.
53	IC (TO-3)	8526	3	0	0
78	TRANSISTOR (TO-5)	8505	5	2	0
79	TRANSISTOR (TO-5)	8445	1	0	0
		TOTAL	9	2	0
		% PASSING	60	13	0

TABLE IX: SOLDERABILITY RESULTS - AU OVER NI, KOVAR, OR ALLOY 42

ID	PART TYPE	DC	SOLDERABILITY NUMBER PASSED/5 TESTED 1 HR.	8 HR.	16 HR.
20	VAR. RESISTOR	8528	5	2	1
21	VAR. RESISTOR	8445	3	1	0
64	IC (TO-39)	8440	1	1	0
		TOTAL	9	4	1
		% PASSING	60	27	7

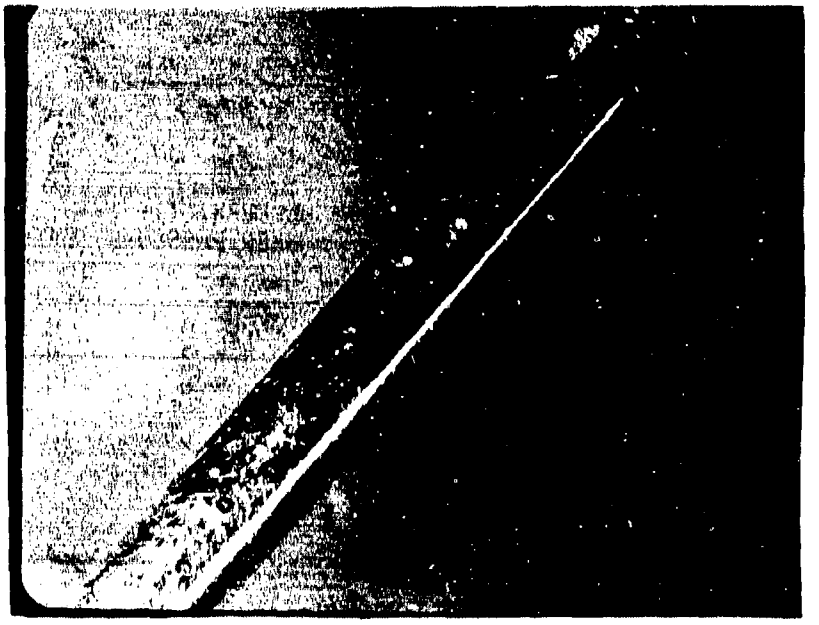


FIGURE 1 - Resistor lead consisting of solder over copper exhibiting acceptable solderability after 1 hour steam aging.

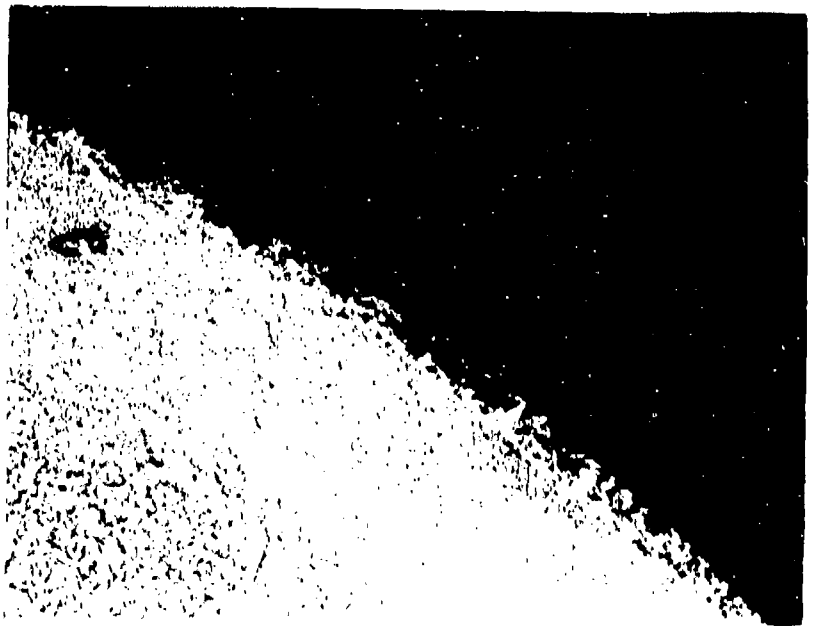


FIGURE 2 - Cross-section of resistor in Fig. 1 which exhibited acceptable solderability after 1 hour steam aging. (1000X)

FIGURE 3 - Resistor lead exhibiting poor solderability after 8 hour steam aging. This part was from the same sample lot as the lead shown in Figures 1 and 2.

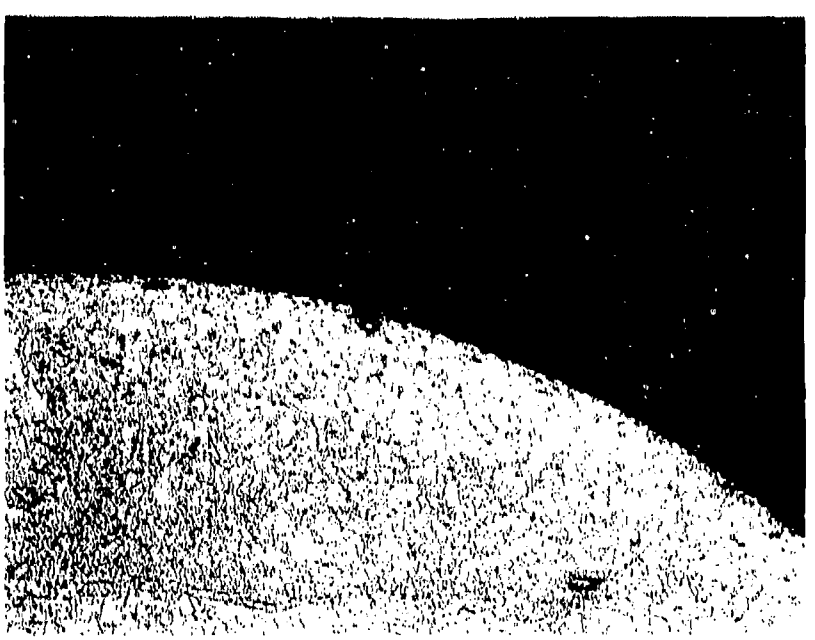


FIGURE 4 - Cross-section of the resistor lead in Fig. 3 showing dewetting after 8 hour steam aging. (500X)

FIGURE 5 - IC lead consisting of tin-lead over Kovar that exhibited good solderability after one hour steam aging.

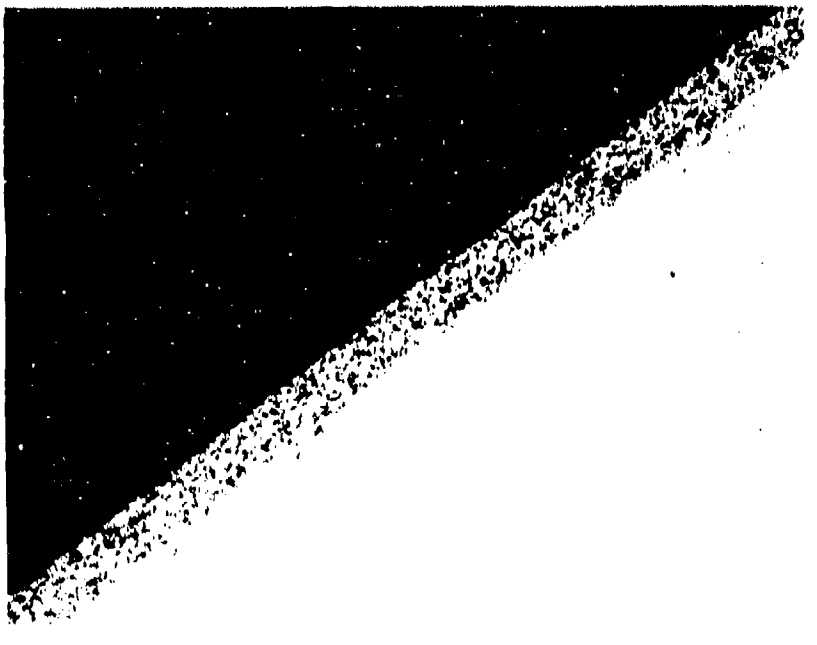


FIGURE 6 - Cross-section of IC lead in Fig. 5 showing condition of solder coat over Kovar base metal. (500X)

FIGURE 7 - IC lead consisting of tin-lead over Kovar exhibiting poor solderability after 8 hour steam aging. This part was from same sample lot as the lead shown in figure 5.

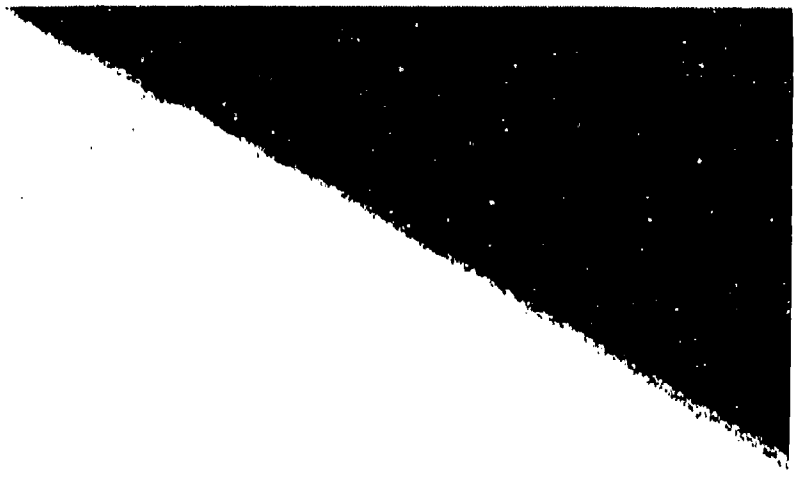


FIGURE 8 - Cross-section of IC lead shown in Fig. 7, showing areas of dewet. (500X)

FIGURE 9 - A variable resistor lead consisting of gold over nickel, exhibiting poor solderability after 8 hours.

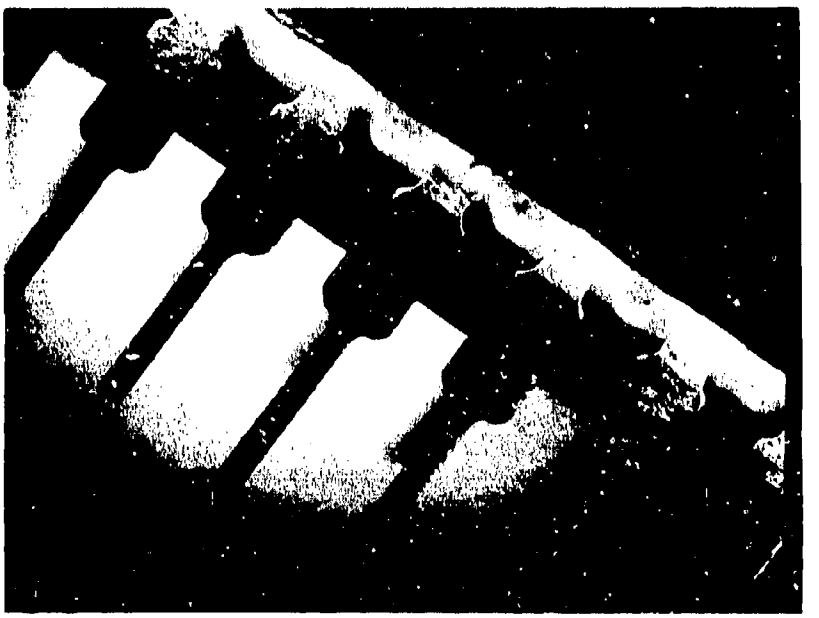


FIGURE 10 - IC leads consisting of solder over Kovar, exhibiting poor solderability after 8 hour steam aging.

FIGURE 11 - Resistor lead consisting of solder over copper that exhibited poor solderability after 16 hours steam aging.

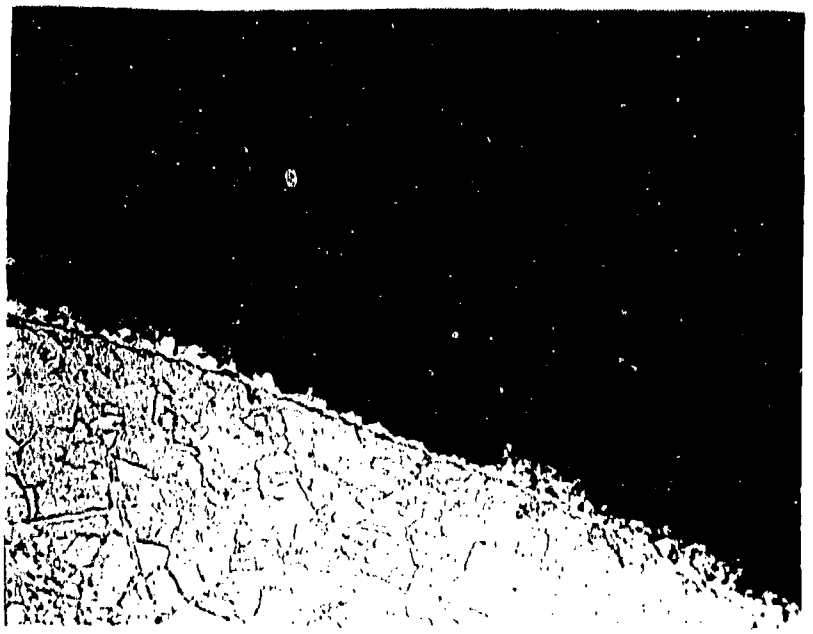


FIGURE 12 - Cross-section of resistor lead in Fig. 11 showing areas of dewet due to exposed intermetallics. (1000X)

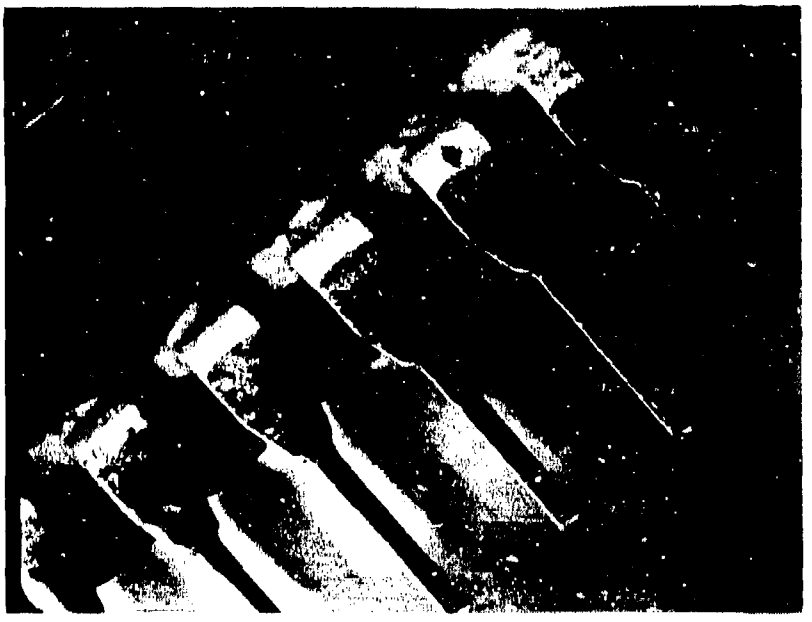


FIGURE 13 - IC lead consisting of solder over Kovar that exhibited acceptable solderability after 16 hours.

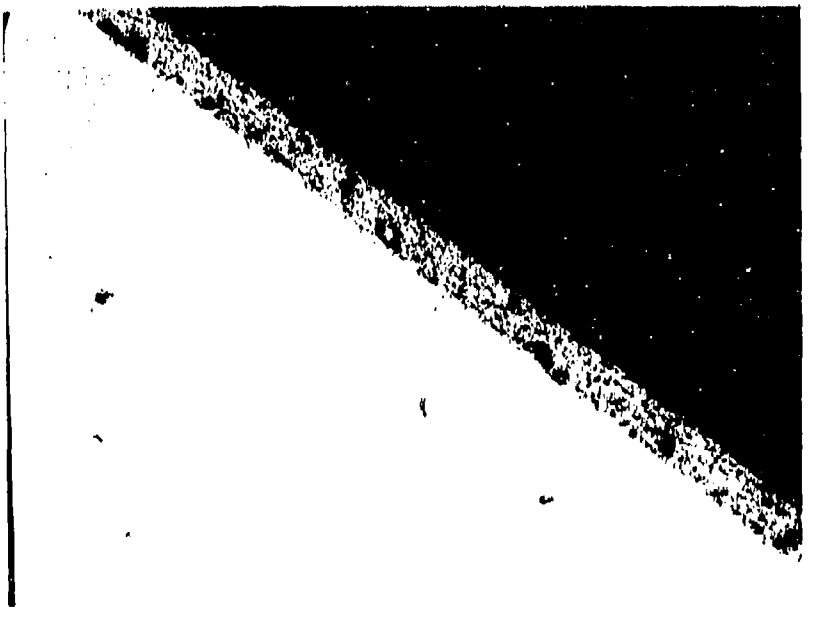
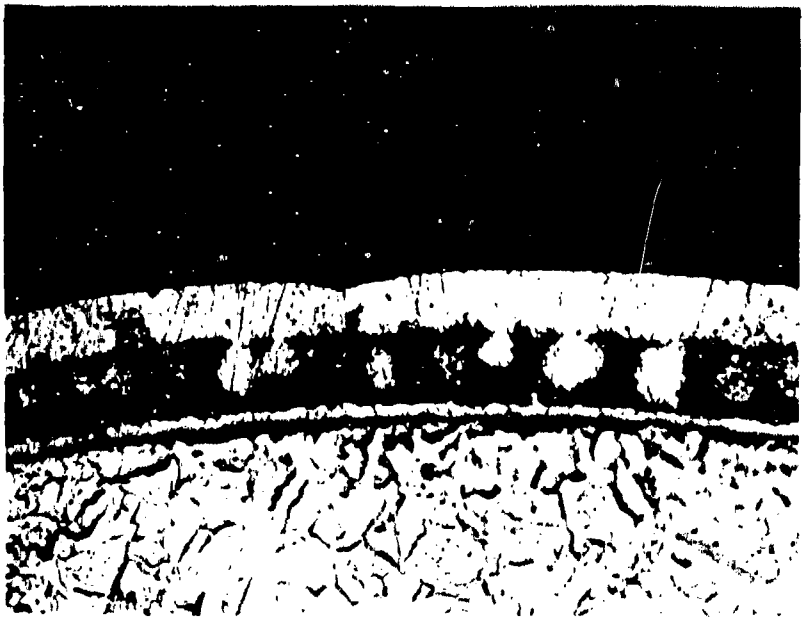


FIGURE 14 - Cross-section of IC lead shown in Fig. 13 showing condition of solder coat after the test.

FIGURE 15 - These two photographs show opposite sides of one cross-section on a copper clad steel capacitor lead having a tin-lead coating. The capacitor manufacturing processes caused a thick build-up of intermetallics. An attempt at rework was made, but the hot solder dip did not completely dissolve the Cu_3Sn layer on one side of the lead. This caused a subsequent dewet problem during flow soldering. (1000X)

FIGURE 16 - Two photographs showing the varying conditions in which leads have been received on incoming parts. (1000X)



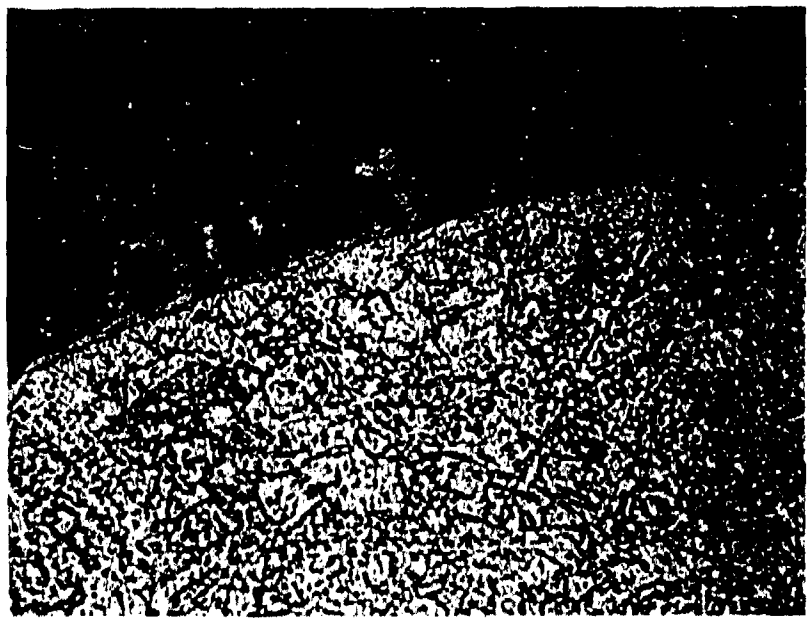


FIGURE 17 - Cross-section of a capacitor lead in as-received condition, showing thick intermetallic layer resulting from the capacitor manufacturing processes. (1000X)

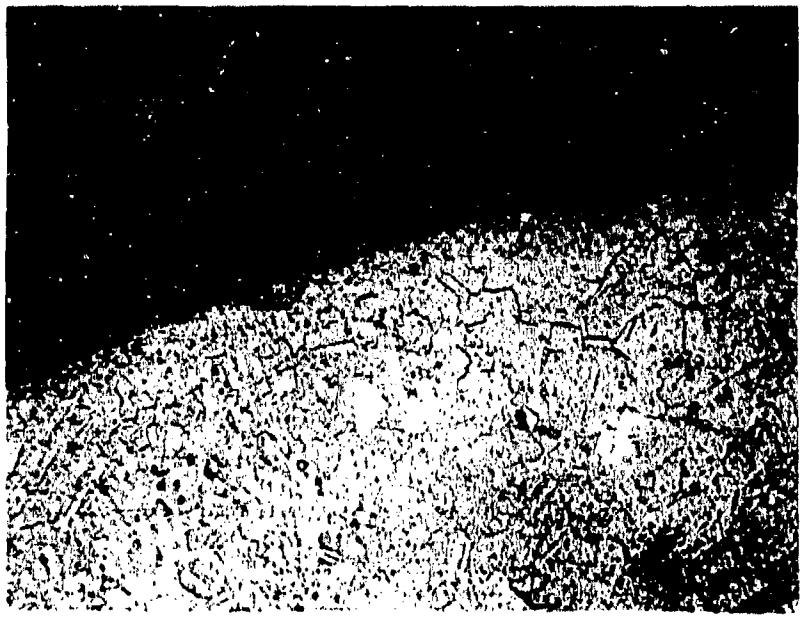


FIGURE 18 - A cross-section of the other lead from the same capacitor, after hot-tin dip, showing that the intermetallic layers were removed. (1000X)

II. CORRELATION OF ACCELERATED AGING TESTS AND ROOM TEMPERATURE STORAGE

Component users want an incoming test that adequately screens out marginal components without being overly demanding of component suppliers. Therefore, experiments and calculations were carried out that directly correlate accelerated aging times with room temperature storage times. Also determined were the aging mechanisms that occur in different aging environments. This first study focused on the tin-lead-on-copper system.

The two subsystems analyzed were 1) dry aging (i.e. oven baking) of 60/40 tin-lead plated copper leads and 2) 90-100% relative humidity aging and dry aging of copper leads coated with 63/37 tin-lead by the dipping procedure as described in MIL-STD-202F, Method 208E. It was suspected that the primary aging mechanism in the first subsystem would be solder consumption by copper-tin intermetallic compound (IMC) formation. The aging mechanism of the second subsystem was suspected to also include solder consumption by oxidation of the solder surface exposed to moisture in air as shown in Figure 18A. Therefore, we characterized the aged specimens with photomicrographs to show IMC thicknesses, and with Auger spectroscopy to measure oxide thicknesses below the solder surface. Five samples per test group were also redipped using an R flux and visually inspected at 10X to 20X magnification for solderability, using the pass/fail criteria of MIL-STD-202F.

The electroplated copper leads were 22 gauge copper wire with 440 microinches of plated solder. The solder was not fused. Figure 19 shows how Cu_3Sn and Cu_6Sn_5 intermetallics grew over time at 150 C. This figure implies IMC formation by Fickian diffusion, since the curves are approximately parabolic, and from Fick's Law,

$$(1) \quad D = L^2 / t,$$

where D is the diffusivity (i.e. diffusion constant), L is the diffusion length (i.e. the solder thickness consumed in aging), and t is diffusion time. For a given aging environment, D is constant, and

$$(2) \quad t \propto L^2$$

The solder-dipped copper leads were 20 gauge copper wire with 300 to 400 microinches of original solder thickness. The samples were aged per the test matrix of Table X. IMC data was measured in twelve places per test group. It was found that the control samples (i.e. unaged) and test groups A4 (i.e. 24 hours steam aging) and E4 (i.e. 24 hours at 150 C oven baking) all had average IMC thicknesses of 70 to 75 microinches. The IMC in these groups was Cu_6Sn_5. None

was Cu_3Sn. It was concluded that solder-dipped copper has superior metallurgical stability to solder-plated copper. A brief explanation follows.

It is well known that Cu_6Sn_5 forms between the copper and the solder during soldering, probably by an electrochemical reaction (Ref. 4), where the flux reacts with tin to form tin chloride in the flux, then tin from the tin chloride deposits onto the copper as an intermetallic (Ref. 5). Lead and copper do not form an IMC, so only the tin-copper IMC is formed. When Cu_3Sn forms next to the Cu_6Sn_5, the large lattice mismatch between these two brittle IMCs increases the likelihood of breakage on a microscopic scale. Twenty-four hours of 150 C aging causes Cu_3Sn to form in the electroplated material, but not in the dipped material since the dipped material has a relatively diffusion-resistant microstructure.

There are two reasons for the relative metallurgical stability of dipped material. First, the concentration gradient (i.e. copper next to Cu_6Sn_5 next to solder) is less, and thus the driving force for diffusion is less than in plated material (i.e. copper next to solder). Secondly, less porous, larger and more tightly packed crystals occur with solder dipping than with unfused solder plating (Ref. 6).

The test groups of Table X were solderability tested per the pass/fail standard of Figure 20. The results are shown in Table XI. Only the high humidity environments produced solderability failures. The failures occurred at 8 hours with 100 C aging, but not until 8 days with 60 C aging.

With data at these two temperatures, an extrapolation can be made to obtain the expected time of solderability failure at a third temperature, namely, room temperature (e.g. 22 C). This is possible, since the temperature-dependence of the diffusion constant, D, generally follows an Arhennius-type relationship:

(3) $D = D_{\infty} \exp(-\Delta Ea/kT)$

where D_{∞} is a constant, ΔEa is the activation energy, k is Boltzmann's constant, and T is the absolute temperature of aging, in degrees Kelvin.

Solderability is lost when solder thickness, L, is consumed at any temperature. So from equation (1),

(4) $D \propto 1/t$, and

(5) $D_{100C} / D_{60C} = t_{60C} / t_{100C} = 192 \text{ hours}/8 \text{ hours} = 24$

Also, from equation (3),

(6) $D_{100C} / D_{60C} = \exp\left[(-\Delta Ea)\left(\frac{1}{kT_{100C}} - \frac{1}{kT_{60C}}\right)\right]$

So from (5) and (6),

(7) $24 = \exp[(-\Delta Ea)(-3.744)]$, and

(8) $\Delta Ea = 0.8488$ eV.

This is the activation energy for solder consumption of solder-dipped copper at high humidity.

Similarly,

(9) $D_{60C}/D_{22C} = \frac{t_{22C}}{t_{60C}} = \frac{t_{22C}}{8 \text{ days}} = \exp\left[(-0.8488)\left(\frac{1}{kT_{60C}} - \frac{1}{kT_{22C}}\right)\right]$

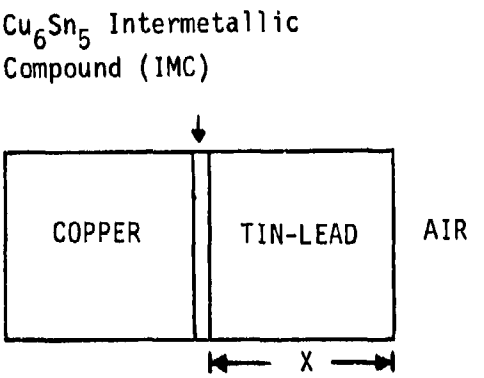
And

(10) $t_{22C} = 8 \text{ days } (45.09) = 360.7 \text{ days}.$

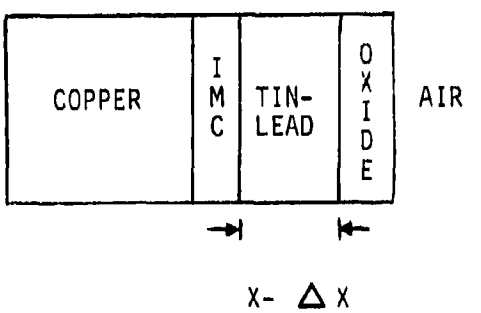
The expected time of solderability failure with room temperature storage of solder-dipped copper is 361 days. Therefore, steam aging for 8 hours correlates with 361 days of room temperature storage in a high humidity warehouse environment. We earlier pointed out the lack of IMC growth with the solder-dipped parts. So what is the mechanism for solder consumption? The Auger results in Figure 21 show that the high humidity of steam aging produces surface oxidation, which does not occur in a 100 C dry environment. This confirms that the aging mechanism model of Figure 18A is correct.

The correlation of accelerated high temperature dry aging with storage in a dry, room-temperature environment follows the same basic procedure. Data on solder-plated copper in Figure 19 shows that 8.9 hours at 150 C produces 40 microinches of IMC. Also, data at room temperature shows that 30 microinches of solder is consumed with one year of room temperature storage (Ref. 7). So the expected time of solder consumption at a third temperature, in a dry environment can be extrapolated. These calculations show that 50 hours of 100 C dry aging correlates with 361 days of dry room-temperature storage. The

AS DIPPED



AGED



Δ X is the amount of solder thickness that is consumed by solid-state-diffusion growth of intermetallic and by oxidation.

FIGURE 18A: AGING MECHANISM MODEL

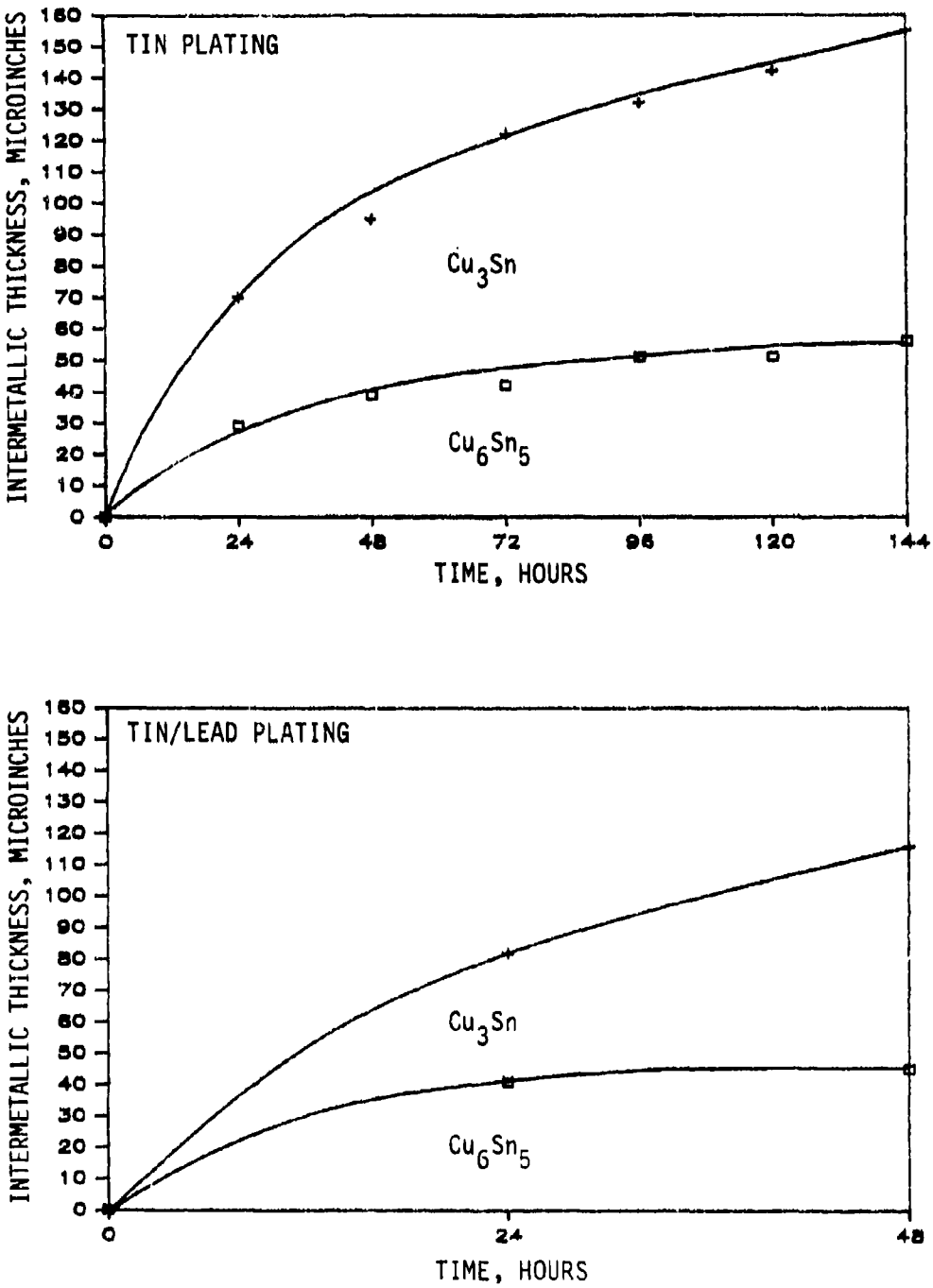


FIGURE 19: INTERMETALLIC GROWTH AT 150°C

TABLE X: AGING TEST MATRIX FOR SOLDER-DIPPED COPPER WIRE

ENVIRONMENT	TIME			
	1	2	3	4
A. 100 C, 100% Relative Humidity (i.e. Steam Aging)	1 Hr	8 Hrs	16 Hrs	24 Hrs
B. 100 C, Dry (<20% RH)	1 Hr	8 Hrs	16 Hrs	24 Hrs
C. 60 C, 90% RH	8 Hrs	24 Hrs	8 Days	11 Days
D. 60 C, Dry	8 Hrs	24 Hrs	8 Days	11 Days
E. 150 C, Dry	1 Hr	8 Hrs	16 Hrs	24 Hrs

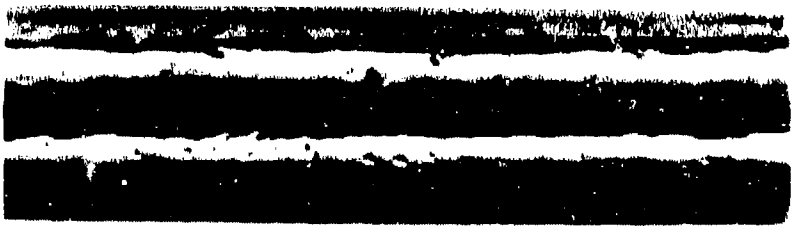


Figure 20 - Figure 208-7 of MIL-STD-202, Method 208

TABLE XI: SOLDERABILITY TEST DATA

TEST GROUP(*)	SAMPLES PASSED/SAMPLES TESTED
CONTROLS (NOT AGED)	5/5
A1	5/5
A2	1/5
A3	1/5
A4	0/5
B1	5/5
B2	5/5
B3	5/5
B4	5/5
C1	5/5
C2	5/5
C3	3/5
C4	3/5
D1	5/5
D2	5/5
D3	5/5
D4	5/5
E1	5/5
E2	5/5
E3	5/5
E4	5/5

* Looking at Table X, C3 would be 60 C, 90% RH for 8 days.

TEST GROUP	OXYGEN ATOMIC PERCENT AT A DEPTH OF 900 ANGSTROMS	1800 ANGSTROMS
CONTROL	0	0
A1	39.2	24.8
A2	25.4	9.0
A4	35.6	35.8
B1	0	0
B2	0	0
B4	0	0

FIGURE 21A: AUGER SPECTROSCOPY OXYGEN DATA SHOWING RELATIVE AMOUNTS OF SOLDER SURFACE OXIDATION

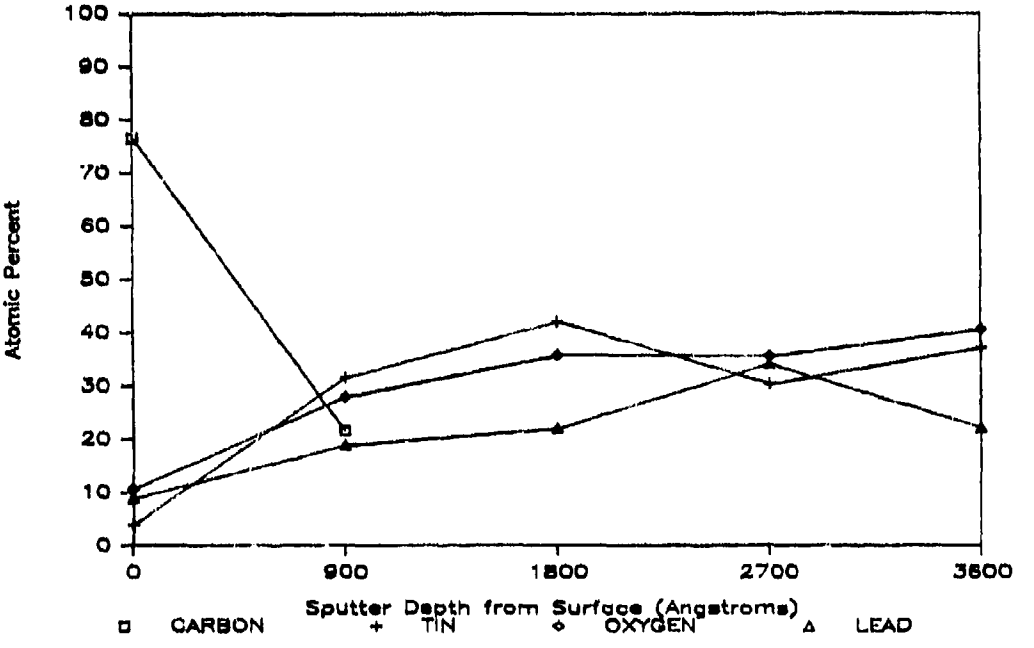


FIGURE 21B: TYPICAL AUGER DEPTH PROFILE

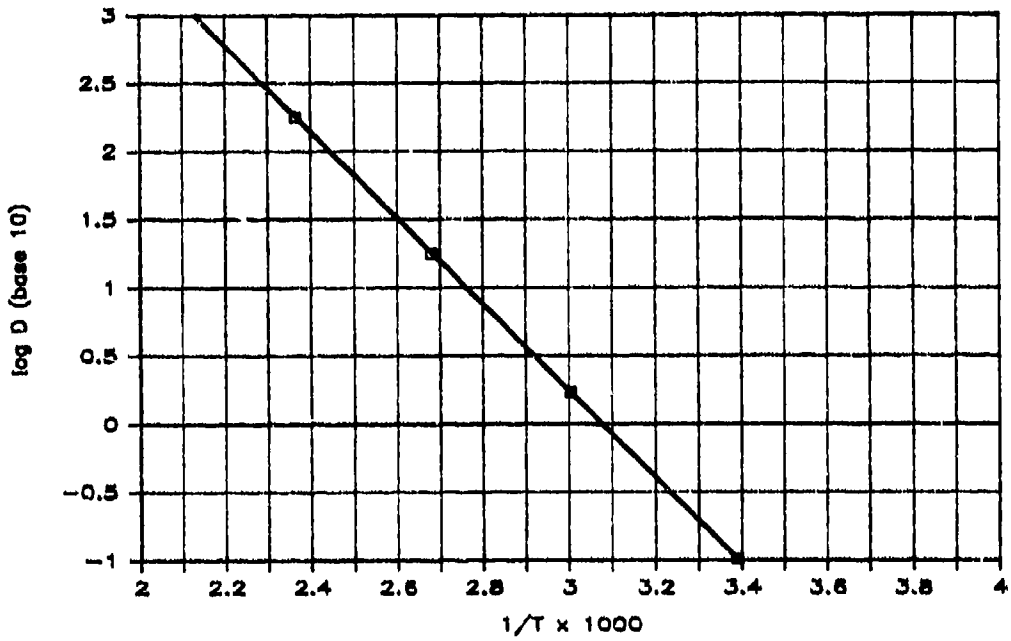


FIGURE 22: ARHENNIUS PLOT FOR DRY AGING OF ELECTROPLATED SOLDER ON COPPER

activation energy here is relatively low, 0.6266 eV, because it takes less energy to activate IMC growth in an electroplated part than in a dipped part.

The diffusion constants, expressed in microinches squared per hour, for various temperatures are: 179 at 150 C, 17.9 at 100 C, 1.71 at 60 C, and 0.103 at 22 C. An Arhennius plot, showing the diffusion constant as a function of any temperature is shown in Figure 22.

This section has illustrated one method to correlate accelerated aging tests with room temperature storage. Specific correlations have been calculated, namely, 8 hours of steam aging corresponds to the same loss of solderability as about one year of high-humidity, room- temperature storage, for solder-dipped copper leads. This initial finding can be verified by experiments and calculations similar to those described in this section, as well as by long-term storage tests.

III. STRANDED WIRE

In mid-1984, TI found itself rejecting 60% of the incoming tin plated, stranded wire because of solderability failures. An extensive effort was undertaken to correct that situation by working closely with the wire manufacturers. As part of the larger TI vendor reduction plan, the number of wire vendors was cut, allowing for more efficient communication with those vendors able to supply the majority of TI's wire requirements. Many lessons were learned.

First, it was found that, like other components, stranded wire is made in several steps by two or three different companies. Second, it became apparent that the Mil-Specs governing stranded wire were inadequate since they did not require a minimum plating thickness on tin plated wire and often did not require solderability testing. The final lesson learned applies well to the theme of this paper. In visiting the vendors' facilities, insight was gained into what was or was not possible for them to do. In turn, it was then possible to offer suggestions and corrective actions. As a result of these efforts, the rejection rate is now only 6% at Incoming Inspection.

SUMMARY

Solderability tests on a representative sample of the most common parts stored in the warehouse indicate that half would not pass the MIL-STD-202F, Method 208E test at this point. This indicates

that the one hour steam aging test currently performed is not an adequate incoming solderability screen to allow storage times up to 1 year in the warehouse. Leads having tin or tin-lead over copper, or gold over nickel performed best both at one and eight hour aging times. Again, finely tuned soldering processes, the tinning of components, and the use of more active fluxes prevent us from seeing problems of this magnitude at the board assembly level.

In order to better explore what aging time would be adequate, another study was made to more closely examine the exact mechanisms that occur in different aging environments. Dry aging of solder-plated copper produced intermetallic compound growth. High-humidity aging of solder-dipped copper produced solder surface oxidation. Solder consumption rates and activation energies were calculated from experimental data. These calculations show that 8 hours of steam aging corresponds to the same loss of solderability as about one year of high-humidity, room-temperature storage, for solder-dipped copper leads. This conclusion is considered a preliminary, initial finding that should be reconfirmed with extensive empirical data before it is generally applied.

Care must be taken not to prematurely insist on more stringent solderability specifications. First, a determination must be made of what is needed and what is possible. Improvements in lead solderability can only be made with a more detailed knowledge of the exact plating systems involved and by determining the exact effect that all subsequent manufacturing steps will have on these materials; from initial lead forming through component assembly, storage and assembly into the system. The solderability of the lead plating system can then be optimized by compensating for or eliminating those processes that cause deleterious effects.

Similar to the familiar situation with leaded components, 1 hour appears to be an insufficient steam aging time for incoming inspection of surface mounted components. Solderability is presently a major problem with surface mounted components (Ref. 8). Another key reliability factor for surface mounted electronic assemblies is the coefficient of thermal expansion (CTE), not just the different CTEs of the device and the substrate, but also of the solder itself (Ref. 9). The high solder CTE can be the driving force for metallurgical instability of surface mounted assemblies.

Future tests are planned to correlate accelerated aging with room temperature storage for plating systems other than tin-lead over copper. Additionally, further aging studies on actual components are planned, including surface mounted devices. Test plans will consider storage conditions and the extent to which solderability test results correlate with actual component-to-board solderability.

CONCLUSIONS

Extensive aging, lead characterization, and solderability testing have shown that certain classes of parts would not solder well. We have studied component leads and how they are handled and have found a considerable risk that large numbers of components will not pass 8 hour steam aging.

As the 8 hour requirement comes into force, there will be two effects. A sudden disruption of the industry may occur and would continue until the older, poorly solderable components are flushed out of the system. Next will begin the era we have worked toward for years; the era in which no components will be sold that do not solder well as stored and used by industry.

This is the conference at which we should sound the clarion to alert component makers and users to the risk that faces them. Everyone should learn from the example set by the IC industry 4 years ago when DESC changed Mil-M-38510 and required the reflow of all IC leads. The IC industry chose to ignore the impact of the DESC order on component solderability. That action on the part of the IC industry cost substantial amounts of money in terms of yield and rework. If the component makers and users do not prepare in advance for 8 hours of steam aging, the results will be similar and we will have no one to blame but ourselves.

ACKNOWLEDGEMENTS

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APPENDIX

AGING STUDY TEST RESULTS
TESTING DATA

ID	PART TYPE	MFR	DATE CODE	SOLDERABILITY TESTING NUMBER PASSED/5 TESTED 1 HR.	8 HR.	16 HR.
1	TANTALUM CAPACITOR	A	8320	5	5	4
2	TANTALUM CAPACITOR	B	8250	4	2	2
3	POLYCARB CAPACITOR	C	8438	4	2	2
4	POLYCARB CAPACITOR	A	8434	5	4	5
5	POLYCARB CAPACITOR	B	8438	3	2	1
6	RESISTOR	D	8449	5	4	2
7	RESISTOR	D	8505	5	4	4
8	CERAMIC CAPACITOR	E	8545	5	3	0
9	CERAMIC CAPACITOR	E	8518	4	0	1
10	RESISTOR	F	8530	5	5	0
11	RESISTOR	F	8325	5	5	5
12	RESISTOR	G	8401	5	3	0
13	RESISTOR		8343	3	3	0
14	MICA CAPACITOR	H	8523	5	3	0
15	MICA CAPACITOR	I	8542	5	2	5
16	TANTALUM CAPACITOR	B	8516	5	1	5
17	TANTALUM CAPACITOR		8541	5	2	2
18	RESISTOR	J		0	0	1
19	RESISTOR	Y	8414	4	5	2
20	VAR. RESISTOR	J	8528	5	2	1
21	VAR. RESISTOR	J	8445	3	1	0
22	RESISTOR	K	8348	5	5	5
23	RESISTOR	F	8503	5	0	5
24	RESISTOR	F	8443	5	2	3
25	RESISTOR	F	8446	0	0	0
26	RESISTOR	L	8327	0	0	0
27	VAR. RESISTOR	M	8109?	0	0	0
28	RESISTOR	F	8416	5	0	2
29	RESISTOR	F	8439	4	0	0
30	DIP IC	N	8437	0	0	0
31	DIP IC	O	8511	5	3	2
32	DIP IC	P	8448	0	1	0
33	IC (TO-3)	P	8216	0	0	0
34	DIP IC	P	8505	2	0	0
35	DIP IC	O	8438	4	5	4
36	DIP IC	Q	8519	1	0	0
37	DIP IC	N	8232	1	2	1
38	DIP IC	O	8311	0	0	0
39	DIP IC	R	8446	2	3	4
40	DIP IC	S	8423	0	0	0
41	DIP IC	T	8442	5	3	4
42	DIP IC	N	8412	2	0	0

APPENDIX (CONT)

AGING STUDY TEST RESULTS
TESTING DATA

ID	PART TYPE	MFR	DATE CODE	SOLDERABILITY NUMBER PASSED/5 TESTED 1 HR.	8 HR.	16 HR.
43	DIP IC	O	8516	5	0	0
44	DIP IC	N	8416	0	0	0
45	DIP IC	P	8442	1	0	0
46	DIP IC	S	8522	0	0	0
47	DIP IC	O	8436	5	0	2
48	DIP IC	O	8502	5	5	5
49	DIP IC	P	8429	5	2	0
50	DIP IC	S	8303?	4	0	0
51	DIP IC	O	8505	5	0	0
52	DIP IC	S	8430	3	1	1
53	IC (TO-3)	P	8526	3	0	0
54	DIP IC	N	8520	2	0	0
55	DIP IC	U	8537	5	5	4
56	DIP IC	V	8503	0	0	0
57	IC (TO-99)	S	8009	0	0	0
58	IC (TO-99)	N	8424	5	4	4
59	DIP IC	O		5	2	1
60	IC (TO-39)	N	8525	5	5	5
61	IC (TO-39)	N	8342	5	5	5
62	IC (TO-3)	N	8505	0	0	0
63	IC (TO-99)	W	8530	5	3	2
64	IC (TO-39)	P	8440	1	1	0
65	IC (TO-39)	P	8435	4	5	3
66	IC (TO-99)		8315	1	0	0
67	IC (TO-99)	P	8510	5	5	5
68	TRANSISTOR	X	8509	0	0	0
69	DIODE	X	8520	5	4	4
70	DIODE	X	8444	5	5	4
71	TRANSISTOR	S	8428	5	4	1
72	DIODE		8516	5	5	3
73	DIODE	X		4	5	0
74	DIODE	X	8525	4	5	4
75	DIODE		8407	4	5	1
76	DIODE	S	8441	5	5	5
77	DIODE	S	8525	4	5	3
78	TRANSISTOR (TO-5)	S	8505	5	2	0
79	TRANSISTOR (TO-5)	S	8445	1	0	0
80	DIP IC	P	8425	5	0	0
81	DIP IC	P	8504	1	0	0
82	DIP IC	N	8427	5	0	0
83	DIP IC	W	8534	5	5	0
84	DIP IC	W	8509	5	0	1
85	DIP IC	P	8431	0	0	0

APPENDIX (CONT)

AGING STUDY TEST RESULTS
PLATING DATA

ID	PART TYPE	MFR	BASE METAL	SN OR SN/PB AVE	SN OR SN/PB MIN	IM AVE.	AU AVE.	NI AVE.
1	TANTALUM CAPACITOR	A	NI,42	284	231			
2	TANTALUM CAPACITOR	B	NI,42	332	300			
3	POLYCARB CAPACITOR	C	CCS	191	72			
4	POLYCARB CAPACITOR	A	CCS	393	249	93		
5	POLYCARB CAPACITOR	B	CCS	433	219	150		
6	RESISTOR	D	CU	835	735	59		
7	RESISTOR	D	CU	769	702	78		
8	CERAMIC CAPACITOR	E	CU	431	339	106		
9	CERAMIC CAPACITOR	E	CU	461	375	39		
10	RESISTOR	F	CCS	497	300	43		
11	RESISTOR	F	CCS	253	195	33		
12	RESISTOR	G	CU	525	315	98		
13	RESISTOR		CU	338	246	138		
14	MICA CAPACITOR	H	CCS	407	255	98		
15	MICA CAPACITOR	I	CCS	364	153	17		
16	TANTALUM CAPACITOR	B	NI,42	25				
17	TANTALUM CAPACITOR		NI,42	282	225			
18	RESISTOR	J	CU	197		98		
19	RESISTOR	Y	CU	247	189	78		
20	VAR. RESISTOR	J	NI,42				28	
21	VAR. RESISTOR	J	NI,42				23	
22	RESISTOR	K	NI,42	454	255			
23	RESISTOR	F	CU	401	369	118		
24	RESISTOR	F	CU	321	249	28		
25	RESISTOR	F	CU	958	699			
26	RESISTOR	L	CU	265	159	37		
27	VAR. RESISTOR	M	NI,42	200	96			
28	RESISTOR	F	CU	342	246			
29	RESISTOR	F	CU	493	396	27		
30	DIP IC	N	42	232	207			
31	DIp IC	O	42	593	525			
32	DIP IC	P	42	243	118			
33	IC (TO-3)	P	NI,42	540	300			
34	DIP IC	P	42	181	71			
35	DIP IC	O	42	330	247			
36	DIP IC	Q	42	1305	77			
37	DIP IC	N	42	674	359			
38	DIP IC	O	42	181	106			
39	DIP IC	R	42	726	649			
40	DIP IC	S	42	100	59			
41	DIP IC	T	42	386	357			

APPENDIX (CONT.)

AGING STUDY TEST RESULTS
PLATING DATA

ID	PART TYPE	MFR	BASE METAL	SN OR SN/PB AVE	SN OR SN/PB MIN	IM AVE.	AU AVE.	NI AVE.
42	DIP IC	N	42	493	307			
43	DIP IC	O	42	327	188			
44	DIP IC	N	42	148	124			
45	DIP IC	I	42	1118	791			
46	DIP IC	S	42	2748	843			
47	DIP IC	O	42	445	212			
48	DIP IC	O	42	172	83			
49	DIP IC	P	42	251	236			
50	DIP IC	S	42	242	224			
51	DIP IC	O	42	316	129			
52	DIP IC	S	42	386	348			
53	IC (TO-3)	P	42	48	30			263
54	DIP IC	N	42	384	53			
55	DIP IC	U	42	326	212			
56	DIP IC	V	42	120	47			
57	IC (TO-99)	S	NI,42	21	18			
58	IC (TO-99)	N	42				27	252
59	DIP IC	O	42	637	590			
60	IC (TO-39)	N	42				66	269
61	IC (TO-99)	N	42				88	216
62	IC (TO-3)	N	NI,42	38	15			
63	IC (TO-99)	W	42				44	182
64	IC (TO-39)	P	NI,42				29	
65	IC (TO-39)	P	42				71	347
66	IC (TO-99)		NI,42	177	144			
67	IC (TO-99)	P	42				80	120
68	TRANSISTOR	X	NI,42	29	24			
69	DIODE	X	CU	450	57			
70	DIODE	X	CU	575	546	70		
71	TRANSISTOR	S	42				23	176
72	DIODE		CU	507	390			
73	DIODE	X	CU	442	414			
74	DIODE	X	CU	440	408			
75	DIODE		CCS	602	540			
76	DIODE	S	CCS				23	197
77	DIODE	S	42				12	146
78	TRANSISTOR (TO-5)	S	42	774	711	125		182
79	TRANSISTOR (TO-5)	S	42	461	384	101		102
80	DIP IC	P	42	926	129			
81	DIP IC	P	42	390	106			
82	DIP IC	N	42	343	147			
83	DIP IC	W	42	390	212			
84	DIP IC	W	42	490	413			
85	DIP IC	P	42	1489	18			

42 REFERS TO EITHER KOVAR OR ALLOY 42
CCS REFERS TO COPPER CLAD STEEL

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ENHANCEMENT OF COMPONENT LEAD PROTECTIVE FINISHES FOR WAVE SOLDERING

by

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ABSTRACT

Wave soldering process controls, often computerized, have evolved to the point that process variations are negligible. The key obstacle to achieving defect-free assemblies is the wide variability in circuit board and component lead protective finishes. Component lead materials, especially their coatings, are covered in detail. Three situations are discussed which have allowed the variabilities to continue until now.

An intensive metallurgical effort was undertaken to understand the root causes of good and bad solderability, to enable upgrading of the finish and solderability specifications, to provide feedback to the component suppliers, and to build an automated system for providing standardized coatings in the interim. This metallurgical effort used state-of-the-art techniques such as SEM/EDX, SEM line profiling, SEM digital color x-ray mapping, SAM surface analysis, SAM depth profiling, and taper microsectioning.

The results included identification of eight solderability failure modes, identification of seven superior protective finishes, recommended improvements in accelerated aging and solderability testing, recommended incorporation of an upgraded Mil-Std-1276 by all component specifications, and the successful automation of a leadwire solder coating process for taped, spooled axial components.

INTRODUCTION

The early 1980s were marked by vigorous efforts in the defense electronics industry to achieve zero-defect wave soldering. Honeywell, armed with solid technical information presented at several NWC Soldering Technology Seminars plus our own in-house experience, sought to reach that goal on one particular Navy contract. Eliminating defective wave solder joints was figured to save an average of 0.4 cent per joint made for that contract. Savings in 1984 by eliminating touchup labor was calculated to be $1.2 million just in the Minneapolis operations.

What the industry generally has done to reduce defects is to incorporate sophisticated CAM wave soldering equipment to eliminate processing variations and to minimize human intervention. Ideal parameters are determined for each printed wiring assembly and stored in the computer so that each subsequent assembly experiences the identical process. Sensors, servo loops, and computer controls assure that the process is controlled.

The result of improving the process at Honeywell's Underseas Systems Division, for example, has been a lowering of defective solder joints from the percentage level to the parts per million level. Although the progress is striking, the existing defect level shows the elusiveness of the zero defects goal. With optimized processes on state-of-the-art equipment, the limiting factor in achieving perfect soldering is no longer the process but the raw materials (components and circuit boards) input into the wave soldering machine. In other words, the variability that allows the current level of defects exists in the materials and protective finishes of component leads and circuit boards. This paper addresses the finishes on leads only.

Materials and Process Engineering (M&PE) is a support group that serves all Honeywell divisions. Due to production's emphasis on automated electronics assembly, our staff's chemists and metallurgists consult daily on electronic packaging materials and processes. Also, our group is often involved in performing referee solderability tests on component leads to give an impartial interpretation of the degree of wetting. In almost every case, a failure analysis of wetting problems is performed in our labs to provide constructive feedback to the manufacturers. Processes to replate or hot solder dip critically needed components' leads are designed by M&PE as well.

CURRENT LEAD VARIABILITY

These many dozens of failure analyses have uncovered three problems that allow the unacceptable variability in the protective finishes of leads to persist. These three are: (1) the loophole problem, (2) the perishable coating problem, and (3) the subjectivity problem.

The loophole problem is characterized by the wording of the component military specifications themselves. Inconsistent coating composition, quality, and thickness are allowed by these specifications. In a large majority of cases, any material may be the lead's basis metal and any coating may be the so-called "protective finish." For example, Mil-R-39008, covering composition resistors, allows anything to be used so long as "a material is used which will enable the resistor to meet the performance requirements of this specification."

The perishable coating problem can best be illustrated by performing systematic solderability tests every 120 days on a large number of component lots. Honeywell's experience on one contract has been the failure of 15% of the components at each test point. Therefore, solderability of component leads is a very perishable quality and the solderability test must take this into account. The normal practice of putting lots into storage before assembly necessitates an accelerated aging for simulating the storage time. Unfortunately, Mil-Std-202, Method 208 (the premiere solderability test), has an inadequate aging cycle of 1 hour in steam. This suffices only for screening thin tin coatings directly over brass and that is not even a normal set of lead materials. Therefore, even when a component lot passes the Method 208 test, it does not follow that the components will be solderable by the time they reach the wave soldering equipment.

The subjectivity problem is caused by the judgmental nature of Method 208's dip-and-inspect test. The subjectivity of deciding 95% coverage promotes confrontation between parts manufacturers and users. Many manufacturers do not acknowledge dewetting as a rejectable defect. This can be blamed in part on the lack of uniform lighting and optics quality at solderability test stations across the country. A bright incandescent lamp masks many wetting defects as does poor quality 10X optics. Lots failed by users usually fall into the loop of comparing supplier and user test results until the lot becomes critical to production and it is refurbished by the user. Solderability test subjectivity assures that nearly 100% of a manufacturer's lots are delivered, although some are actually in poorly solderable condition.

These three problems allow a tremendous variability in lead protective finish quality. Recent Honeywell R&D work has pointed out similar, perhaps more critical, variations on leadless chip component terminations. These variations are due to the same three problems as listed above for leaded components.

METALLURGICAL STUDY OF LEAD FINISHES

With these problems in mind and NWC's Soldering Technology Branch pushing for a totally automated factory, Honeywell committed over $400,000 in R&D funds toward their resolution. In-depth scientific studies were performed at Honeywell to understand:

1) what protective finishes were being supplied routinely,
2) what caused acceptable or rejectable solderability of these finishes,
3) what the military specifications should require of protective finishes on leads,
4) how to upgrade Mil-Std-202, Method 208, aging and objectivity,
5) what process could be automated to provide a standard, storable coating for leads, and
6) automation of said process.

These studies keyed on understanding the root causes and effects of solderability so that we could improve our suppliers' processes as well as on automating an in-house means of standardizing the leads input to the wave soldering operation.

For the study, 129 component lots were randomly selected at receiving inspection. These lots were solderability tested without steam aging. Leads from each lot were microsectioned as-received and transverse to their axes to allow measurements of the plating and reaction zone thicknesses. This provided important information on good and bad finishes.

Thirty-nine (30%) of the lots failed this solderability test. All 39 failures were analyzed in detail by several of the following state-of-the-art techniques.

Taper (10:1) microsectioning was used to distinguish fine details and defects in the plating and reaction zone layers. Figure 1 is an example of a taper microsectioned resistor leadwire with several problems. The layers from left to right are: (1) the copper wire, (2) the epsilon copper-tin intermetallic, Cu_3Sn, (3) the nu prime copper-tin intermetallic, Cu_6Sn_5, (4) a very lead-rich, tin-lead alloy, and (5) the copper overplate applied by our lab for edge retention. With such a thick, interdiffused copper-tin reaction zone, the original tin-lead alloy protective finish had drastically thinned and had been depleted of tin. The remaining, unreacted coating was too thin to protect the surface of the copper-tin layer and was too lead-rich to melt quickly at normal wave soldering temperatures.

Figure 2 shows an integrated circuit lead taper sectioned to study the porosity in its thin tin plating. The tin's gross porosity and thinness allowed oxidation of the Kovar lead material surface and degraded solderability.

FIGURE 1. Taper Microsectioned Resistor Lead.

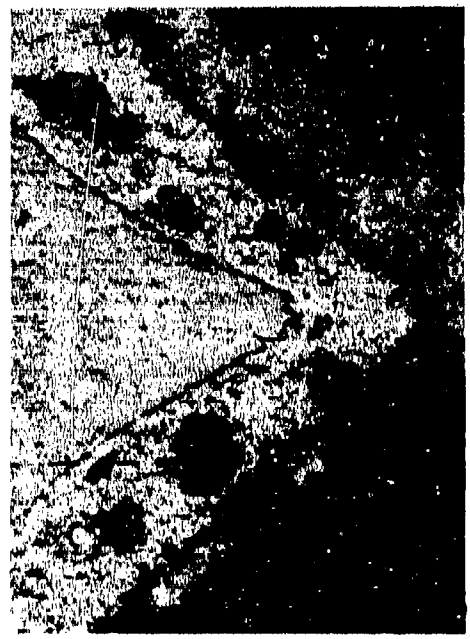

FIGURE 2. Taper Microsectioned IC Lead.

Another very useful tool in performing solderability failure analyses was the scanning electron microscope/microprobe (SEM/EDX). Both the line profiling mode and the digital color x-ray mapping proved to be invaluable in determining why a finish was inadequate for solderability retention. Figures 3, 4, 5 and 6 are SEM micrographs of a nonsolderable transistor lead overlaid with straight horizontal scan lines and jagged spectra showing relative levels of tin, nickel, phosphorus, and iron, respectively. This Kovar lead had been electroless nickel (Ni-P) coated and then thinly tin plated. Solid-state interdiffusion of the tin and nickel was highlighted by this line profiling technique. SEM/EDX spectra also identified high phosphorus levels as contributors to the failure.

Figure 7 is an example of digital x-ray mapping done by the Kevex computer with the SEM. A tin-lead solder joint between a leadless chip capacitor and a silver metalized circuit pad is shown in cross-section. Of course, the black and white reproduction cannot show that the areas composed of silver, nickel, tin-lead, and silver-tin intermetallic were each assigned different colors. However, the color-enhanced map, composed of pixels each made by an EDX scan at a point, allowed the labeling of the various phases in the joint. A thin, silver-tin intermetallic layer was observed between the solder and the printed-wiring board metalization, which was expected. Unfortunately, some dissolution of the capacitor's silver termination was noted through pores in the nickel barrier plating, indicating the barrier's inadequate thickness or density.

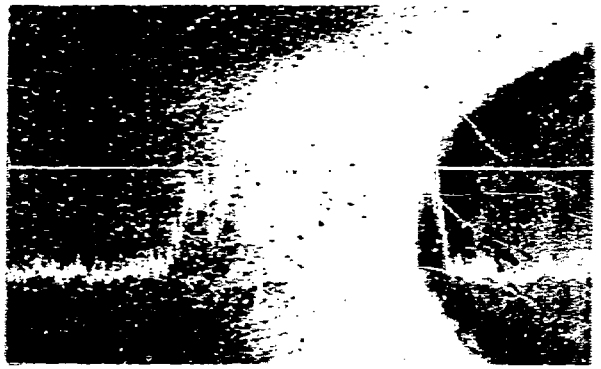

FIGURE 3. SEM Micrograph with Line Profile of Tin Level.

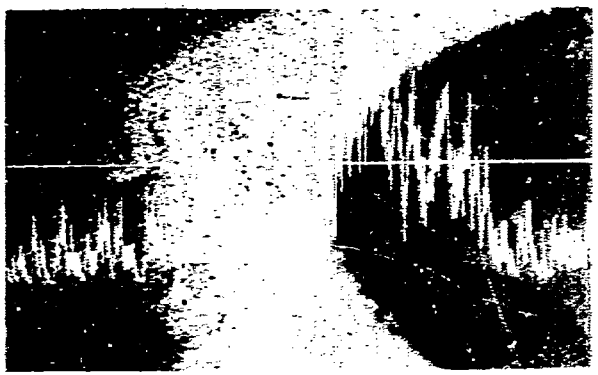

FIGURE 4. SEM Micrograph with Line Profile of Nickel Level.

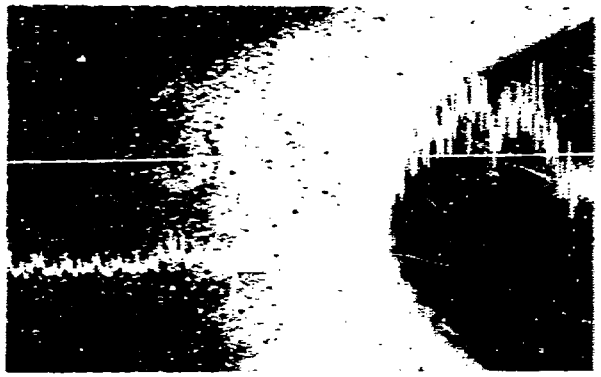

FIGURE 5. SEM Micrograph with Line Profile of Phosphorus Level.

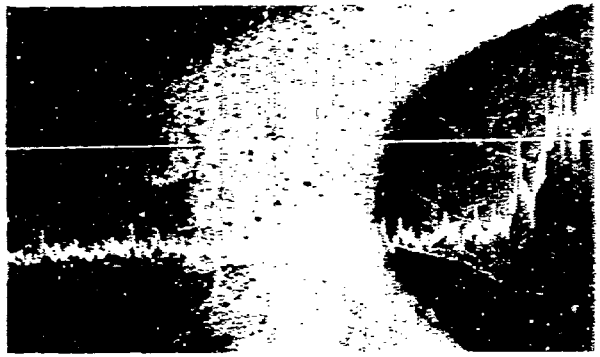

FIGURE 6. SEM Micrograph with Line Profile of Iron Level.

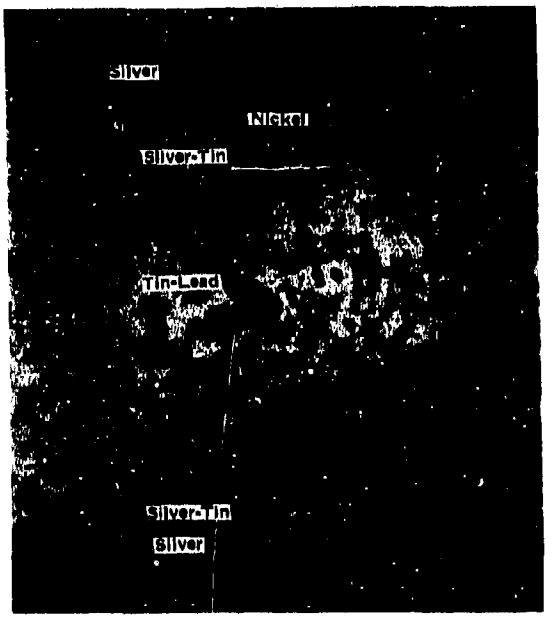

FIGURE 7. SEM Digital X-Ray Map of Solder Joint to Chip Capacitor.

Scanning Auger Microscopy (SAM) is a sensitive surface analysis technique which detects Auger electrons emitted from the outer 10 angstroms of a bombarded surface. This allowed detection of surface contaminants such as unusually high levels of organic material or oxides. Continuous elemental scans, coupled with simultaneous argon ion etching, provide informative depth profiles (composition versus depth scans). Figure 8 represents a typical surface elemental scan whereas Figure 9 shows atomic concentrations versus sputter time (depth). Depth profiling provided information on the depth of diffusion and on contaminants within or under plated layers.

The first result of the metallurgical study was a listing (Table 1) of routinely supplied, component lead protective finishes.

The mix of component lead finishes was no surprise once the applicable military specifications were studied. Table 2, which lists some of the capacitor, resistor, and semiconductor specifications, highlights the fact that almost any coating can be used on a given device and certainly any quality of coating is allowed. Two noteworthy exceptions to this lack of quality were discovered. They are Mil-M-38510 for microelectronics and Mil-Std-1276 for electronic component leads. Mil-Std-1276 is particularly attractive and M&PE will work toward upgrading this standard and having the improved version incorporated by more component specifications.

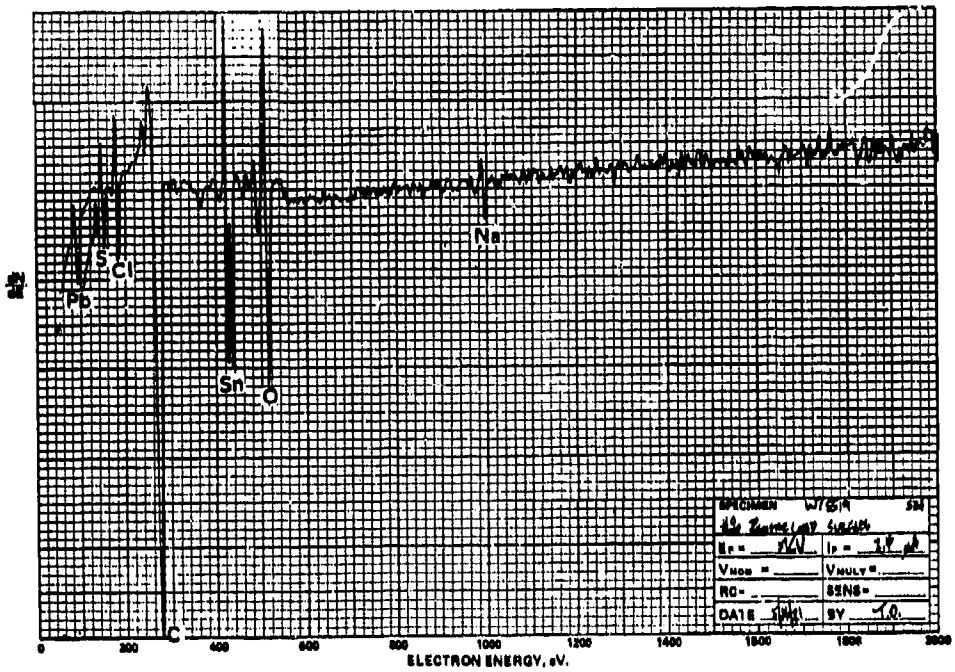

FIGURE 8. SAM Surface Spectrum.

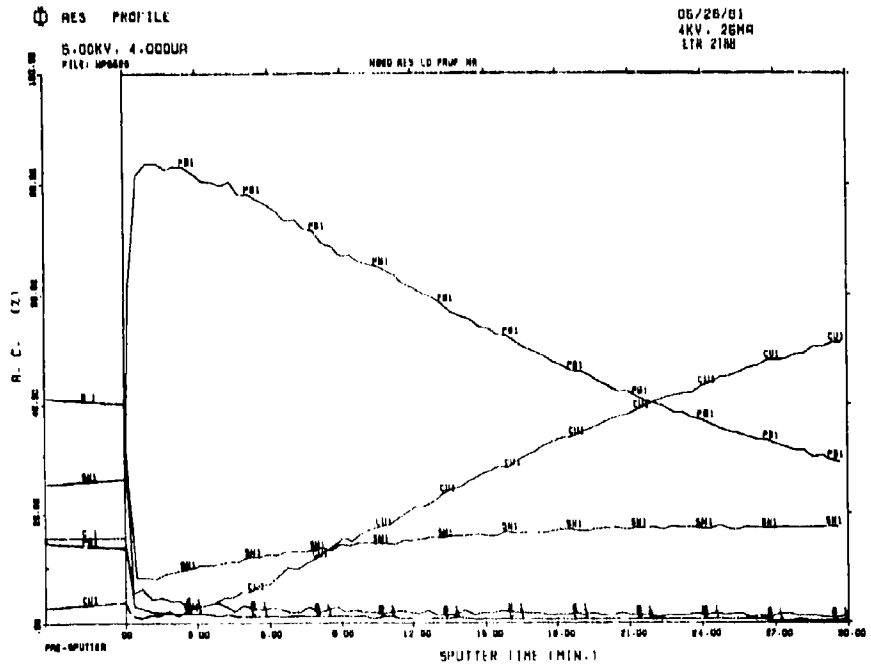

FIGURE 9. SAM Depth Profile.

TABLE 1. Protective Finishes As-Received from Manufacturers.

Thick tin or tin-lead (electrodeposited) over copper, nickel, (nickel substrates ranged from electrodeposited to electroless to the wire itself, or iron-nickel.
Thin tin or tin-lead (electrodeposited) over copper, nickel, or iron-nickel.
Thick tin or tin-lead (hot dip or reflowed) over copper, nickel, or iron-nickel.
Thin tin or tin-lead (hot dip or reflowed) over copper, nickel, or iron-nickel.
Gold flash (less than 8 microinches thick) over nickel or iron-nickel.
Thin gold (less than 50 microinches thick) over nickel or iron-nickel alloy.
Gold (more than 50 microinches thick) over nickel or iron-nickel.
Silver over copper, nickel, or iron-nickel.
Lead over copper, nickel, or iron-nickel.
Zinc over copper.

Results from the 39 failure analyses combined with M&PE's experience allowed solderability failures to be categorized into the eight causes or modes listed in Table 3. Recommended general techniques for enhancing solderability are also listed. Failure analysis for solderability is now a very routine operation in Honeywell's M&PE labs.

These failure modes highlight the perishable nature of normal coatings. A majority of the problems were due to solid state diffusion between the coating and the substrate or environmental degradation of the coating's exterior.

As an additional benefit from the metallurgical study, M&PE was able to determine the superior protective finishes for providing long-term solderability. The finishes in Table 4 have become the basis for callouts on Honeywell purchase orders.

M&PE plated numerous test pieces and tested various accelerated aging and instrumented solderability techniques. The results of accelerated aging allowed us to rate Mil-Std-331 temperature and humidity cycling (28 days) as most severe, dry heat aging (16 hours at 155°C) as severe, IPC's 20- to 24-hour steam aging as optimum, and Mil-Std-202, Method 208, as insufficient. It was obvious that the military's move toward increasing Method 208's aging length to 16 hours will be an improvement. The results of using a laboratory-built surface wetting balance showed the promise of objective solderability testing but also revealed several shortcomings in both our in-house and the commercial instrumentation.

TABLE 2. Military-Specified "Protective Finishes."

Component Type/Spec	Terminal Material and Finish Callouts	Finish Spec/ Thickness Requirements
Ceramic capacitor:		
Mil-C-20	None	None/None
Mil-C-20/35	None	None/None
Mil-C-39014	None	None/None
Mil-C-39014/24	None	None/None
Mil-C-11015	"Terminals shall be coated with solder having a 40 to 70% tin content."	None/None
Mil-C-11015/9	None	None/None
Plastic capacitor:		
Mil-C-55514	"Terminals: Solid conductor suitably treated to facilitate soldering. When a coating containing tin is used, the tin shall range between 40 and 70%."	None/None
Mil-C-55514/2	None	None/None
Supermetalized plastic film capacitor:		
Mil-C-83421	None	None/None
Mil-C-83421/1	Large cases: "Solder-coated, copper-clad steel leads. or "Type N2 of Mil-Std-1276 when specified in p.o."	None/None Mil-G-45204/50-225 microinches or less than 50 microinches
	Small cases: "Type C of Mil-Std-1276."	None/None
Variable, comp resistor:		
Mil-R-94	"Terminals suitably treated to facilitate soldering."	None/None
Mil-R-94/4	None	None/None
Fixed, comp resistor:		
Mil-R-39008	None	None/None
Mil-R-39008/2	None	None/None
Fixed, film resistor:		
Mil-R-39017	"Type C of Mil-Std-1276. Leads free of non-conductive and foreign materials."	None/"Maximum coating thickness less than twice the minimum thickness of any cross section."
Mil-R-39017/2	None	None/None
Variable, wire-wound resistor:		
Mil-R-27208	"Terminals protected by a corrosion-resistant metallic coating and suitably treated to facilitate soldering."	None/None
Mil-R-27208/10	None	None/None
Mil-R-39015	"Terminals suitably coated to meet solderability requirements."	None/None
Mil-R-39015/1	None	None/None

TABLE 2. Military-Specified "Protective Finishes." (Concluded)

Component Type/Spec	Terminal Material and Finish Callouts	Finish Spec/ Thickness Requirements
Semiconductor device:		
Mil-S-19500	None	None/None
Rectifier diode/240	"Lead finish shall be gold-plated, silver-plated, or tinned."	None/None
Power diode/297	None (Note: 15-second dwell time for solderability using Mil-Std-750, Method 2026.)	None/None
Power diode/420	"Lead finish shall be gold, silver, or tinned."	None/None
Low-noise diode/435	"Lead finish: Leads shall be tinned or gold-plated."	None/None
Thyristor/108	None	None/None
Thyristor/276	"Lead finish: Lead material shall be Kovar or Alloy 52. Lead finish shall be gold-or tin-plated."	None/None
Power transistor/315	"Lead material and finish: Lead material shall be Kovar or Alloy 52. Lead finish shall be gold plated, tin plated, or solder dipped."	None/None

A primary benefit of the metallurgical study was usage of the findings to design processes and then equipment for semiautomated and fully automated lead coating equipment. Again, the goal was to provide a standard, storable coating for later defect-free wave soldering. Although either thick electrodeposits or hot dip coatings were proven as equally good coatings, lab tests proved that in-line plating equipment would be much too slow and difficult to design for the large volumes of leads anticipated. Hot solder coating was selected for automation. Taped and spooled axial-leaded devices, the largest volume of components used, were selected as the style of component for which Honeywell would design an automated system.

Such a machine had to be adaptable to all three EIA taping classes and meet both Honeywell internal needs and those for CCAPS. The tape used to package the axial devices had to be left intact during processing and pass through without degrading.

Using the generic processes Honeywell had developed, a prototype was built. It evolved into a 23-foot-long machine which is an in-line system using all the processes needed to fix the majority of lead finish variables (found in our metallurgical study) which allow solderability degradation during storage. The basic system degreases the leads, fluxes both leads with type OA flux, hot solder coats the leads at separate solder waves, cleans the flux residues, and dries the components before respooling.

TABLE 3. Soldering Failure Modes and Techniques for Restoration.

Failure Mode	Restoration Technique
1) Mold release compound, oil, grease, soil at surface	Surface cleaning; solvent, alkaline, fluorocarbon, or aqueous.
2) Zinc, lead, or lead-rich coatings	Strip or dissolve in molten solder at high temperatures.
3) Contaminated tin or tin-lead	Strip, overplate or hot solder dip.
4) Surface oxidation of tin or tin-lead	Brighten or hot solder dip.
5) Thin, porous gold with oxidized substrate	Brighten, overplate, or hot solder dip.
6) Thin, porous tin or tin-lead with oxidized substrate	Brighten, overplate, or hot solder dip.
7) Thin tin or tin-lead with substrate diffused too near surface	Strip, overplate, or hot colder dip.
8) Soluble plating over nonsolderable substrate	Strip and activate or overplate.

TABLE 4. Component Lead Finish Requirements.

Resistor Family (copper or copper alloy leads)	
Finish I:	Matte tin-lead 300 to 600 microinches.
Finish II:	Hot dip tin-lead (Sn60-63) 60 microinches minimum and well wet with minimal time at temperature.
Finish III:	Matte tin 300 to 600 microinches.
Transistor/Diode/IC Family (iron-nickel alloy or Kovar leads)	
Finish IV:	Pure gold 50 to 100 microinches over 100 microinches nickel minimum.
Finish V:	Matte tin 300 to 600 microinches over 100 microinches nickel minimum (tin must be reflowed if Mil-M-38510 part).
Finish VI:	Matte tin-lead 300 to 600 microinches over 100 microinches nickel minimum.
Finish VII:	Hot dip tin-lead (Sn60-63) 60 microinches minimum and well wet over nickel 100 microinches minimum. Minimal time at temperature during hot dipping.

To assure Honeywell and the NWC's Soldering Technology Branch that components were not degraded by the process, an electrical and cleanliness test plan was devised jointly. Honeywell performed the testing which proved that our specific machine yielded an acceptable product and that our quality control testing was adequate for Honeywell use. This was finished in December 1985 and the machine has processed over 1.25 million components for a production contract at up to 20,000 components per hour. The theoretical limitation of a single type of component is 32,000 units per hour.*

This process provides a standard, repeatable finish for EIA classes I, II, and III taped components. It provides in-line cleaning and drying in an optimized time frame. It eliminates costly, error-prone, and sometimes dangerous, manual dipping. Thus, Honeywell has achieved its goal of providing a standardized, storable lead finish on the largest group of components (axial, taped styles) to our optimized wave soldering process. Coupled with M&PE's efforts in circuit board solderability, this will allow wave soldering using type R or RMA fluxes and generation of zero defects.

Fundamental to the success of wave soldering at Honeywell is M&PE's in-depth metallurgical and chemical knowledge of the root causes of good and bad solderability. Because of this knowledge, Honeywell's procurement and quality departments now have real specifications on protective finishes. M&PE can work toward incorporating real requirements into the component specifications, accelerated aging can be upgraded, solderability test objectivity can be improved, and constructive and detailed corrective actions can be provided to our suppliers. A real bonus has been the automation of a system to standardize finishes on our largest group of components.

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* Tests at NWC have not yet been completed.

Mark Shireman is the Principal Metallurgist/Materials and Process Engineer (Soldering Technologist) with Honeywell. He earned a BS degree in Material Science from Northwestern University in 1977 and since that time has been deeply involved in scientific studies of the causes of good and bad soldering, electronic packaging, and vendor interfacing. His work earned him the Honeywell Special Achievement Award in 1984 for solving hand-soldering problems, and Honeywell's top scientific award–also in 1984 for soldering technology. He was the Honeywell Engineering Club's nominee for 1985 "Young Engineer of the Year in Minnesota." In 1985 he was allowed a U.S. patent for co-inventing an Automatic Lead Tinner, which was selected as one of the "Seven Engineering Wonders in Minnesota" in 1986. Mark is a member of the American Society for Metals and is Membership Chairman for the International Metallographic Society.

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WETTING BALANCE SOLDERABILITY TESTING OF ELECTRONIC COMPONENTS AT RECEIVING INSPECTION

by
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COMPONENT LEAD SOLDERABILITY VERSUS ARTIFICIAL STEAM-AGING

by
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QUALITY THROUGH TRAINING

by

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ABSTRACT

Controlling the electronic manufacturing process is the "Quality Insurance Program." Factors to be considered are:

Product
Personnel
Process

This paper addresses the training requirements for operating personnel assigned to the manufacturing area. Having properly trained operators will ensure producing reliable quality products at a competitive cost. To effectively and efficiently train operators, there are basic requirements which must be satisfied. They are:

1. Course Curriculum
2. Training Area Design
3. Instructor Selection
4. Training Program
5. Student Pre-screening
6. Student Stress Control
7. Recertification
8. Special Courses

COURSE CURRICULUM

The course curriculum can only be designed after a thorough basic skills needs assessment study has been conducted. This study will establish and answer the question, "What skills and knowledge must operators have to efficiently produce quality products?"

Basic skills should be separated from the special skills training requirements to ensure having each student trained and tested to an accepted basic skills level.

Special skills training can be scheduled when student has received job assignments on the production floor.

Basic skills requirements:

a) Mechanical assembly
b) Tool use and care
c) Hand wiring and soldering
d) Wave soldering
e) Inspection
f) Touch-up and rework
g) Electro-static discharge (ESD)
h) Orientation and good housekeeping

Some special skills requirements:

a) Cable fabrication
b) Jumper wires
c) Component identification
d) Engineering design changes
e) Printed wiring board repair
f) Surface mount technology
g) Process sheet reading

TRAINING AREA DESIGN

The training area should be designed to provide the student with "a feel" of what an actual production position will be like. The training area position should mirror the actual production position. Ergonomics, biomechanics and human factors are prime considerations in the design of the training area.

Design factors:

a) Work station
b) Seating
c) Lighting
d) Heating/air conditioning
e) Tools and equipment
f) Audio/visuals
g) Materials
h) Quality documentation

The training area should be isolated from regular production noise and pressures to allow the student to learn properly. The concept of quality can be taught much more effectively in a proper training environment.

INSTRUCTOR SELECTION

The selection of the instructor is of primary importance as he is the keystone to the success of the training program. The instructor must have excellent communication skills to ensure having each student understand the information being presented. The old adage still prevails -- "If a student hasn't learned, the teacher hasn't taught." The instructor must also have the required manual skills allowing him to demonstrate the proper wiring and soldering methods and techniques.

TRAINING PROGRAM

A teaching plan must be developed from the course curriculum. The instructor must schedule his time to provide:

a) Lecture/AV presentations

b) Demonstration of methods and techniques

c) Students practicing methods and techniques

d) Students producing workmanship samples

Effective teaching has been predicated on the following axiom for many years.

I HEAR . . . . . AND I FORGET.

I SEE . . . . . AND I REMEMBER.

I DO . . . . . AND I UNDERSTAND.

The course must be segmented into training modules. This allows students to learn skills in a build-on manner. The student must produce workmanship samples for each segment/module. Producing of workmanship samples can be used to promote decision making by the student. The instructor will evaluate the first samples and offer corrective recommendations for the student's benefit. All subsequent samples will be evaluated by the student, who will compare the sample to a workmanship manual and make a workmanship assessment. The instructor then evaluates the student's quality assessment. He can then accept the sample or offer corrective recommendations. This student decision/instructor interface will prepare the student for actual quality decisions on the production floor. This practice will definitely reduce touch-up and operator/inspection indecision on the production floor.

The practice of having students produce workmanship samples for each segment/module taught will provide the instructor/company a visible record of student's comprehension/skill level. The continual assessment provides necessary data for determining student's progress. This data permits deciding whether:

a) Student's performance is satisfactory

b) Additional training is recommended

c) Student is not capable of performing assigned task and should be reassigned or terminated

At the end of the course, each student must have a package of approved workmanship samples for each module/segment.

A written test must also be taken by each student to measure comprehension level of course material presented. The workmanship samples and the written test eventually become a permanent part of the student's employee file/record. Satisfactory completion of the training course should culminate in a formal presentation of completion certificate and a certification card duly authorized by the instructor.

EMPLOYEE/STUDENT PRE-SCREENING

Pre-screening and testing of prospective applicants has become increasingly important. The "new electronics" utilizing micro/macro componentry and high density packaging has introduced new requirements into our labor force.

Basic pre-screening requirements are:

a) Eyesight examinations

b) Language understanding

c) Comprehension testing

d) Acceptable manual dexterity

e) Attitude (sparkle-in-the-eye)

STUDENT STRESS CONTROL

The instructor's primary concern is the transfer of knowledge to the students. The best way to reduce stress in the training room is to know your students. The more you know about them, the more you can understand the stresses they may be experiencing. The person may be out in the work force for the first time, out of necessity, or just wanting to work.

You must consider the environment the student is coming from and the new experiences the student is undergoing. The more understanding given the student, the greater the response, resulting in a better employee.

Some factors the instructor should consider are the student's:

a) Background -- previous experience and training

b) Education

c) Present skills level

Stress considerations are also very important during the student's first interface with the production area. The student now interfaces with a new environment, actual production material, production effort (schedule), other employees (peers), and first line supervision.

In spite of all of the above, it must be repeatedly conveyed to the student, as a prospective new employee, that performing quality work at the assigned tasks is an integral part of the overall company work effort. Quality is a state of mind, not just a production objective.

RECERTIFICATION

Recertification, or continual skills assessment on the manufacturing floor, must be scheduled and controlled. The recertification schedule must be established based on factors such as:

a) Quality level

b) Complexity

c) Criticalness

d) Cost

Recertification is a mandatory process in that operators quickly develop work shortcuts on the manufacturing floor that, in many instances, are in contradiction with time proven methods taught in the classroom.

SPECIAL COURSES

INSPECTION TRAINING

Inspectors must be thoroughly familiar with the company's workmanship specification and workmanship manual. The reason for rejection of any solder connection or electronic hardware must be substantiated by the documents. This technique promotes recognition of all classic rejects by sight and thorough understanding of the written criteria in the specification. This will

reduce touch-up and rework. The doctrine of acceptance based on functionality, not aesthetics, must be pursued to reduce touch-up.

Inspectors must be trained by using actual samples or color photography criteria showing exactly what is required. This means positive establishment of preferred, minimum, and maximum acceptance criteria.

A formal inspection testing program must be designed and implemented. Recertification of inspectors must be done on a regular basis to ensure uniformity of the inspection function. Continual retraining and assessment of inspection skills through recertification must be scheduled. This process will reduce indecision and opinion calls by inspectors which could result in costly rework and/or possible scrapping of expensive electronic hardware.

Most successful companies have made the satisfactory completion of the hand wiring and soldering course a prerequisite of the inspection course.

CONCLUSION

Cost effective production of quality products can only be achieved by proper selection and training of operators by qualified instructors using industry accepted methods and training materials.

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PROPOSED STANDARD FOR "MAGNIFYING POWER" OF VISUAL MAGNIFICATION AID/DEVICES AND "HUGHES MAGNASCOPE" CALIBRATION INSTRUMENT DESCRIPTION AND USE

by

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ABSTRACT

PROBLEM: Many magnification aids have magnifying power values advertised, specified, and stamped on them, but it seems that almost everything but standard microscopes are incorrectly marked and do not conform to any recognized optical equation for determining magnifying power. We found almost all 4X inspection devices ran from 0.8X to 3X, and 10X devices ran from 5.6X to 11X; also three very complex, very expensive instruments were all about one-half their marked value.

HAND HELD SOLUTION: Because of this, Hughes has designed and built special wide-angle, low distortion, high resolution, long-working distance, 4X and 10X magnifiers mounted in the center of fiber optics ring lights which are hand held or mounted on a swivel-swing arm stand.

ADVANCED INSTRUMENT SOLUTION: Hughes has also designed and is building a special "Optical Semiautomatic Inspection Station." This new system utilizes a stereo head-up display with large pupils, long eye relief, wide field, high resolution, coplanar objects, optimized toe-in and eye focus distance, is computer driven, and features low fatigue, and fast operating concepts.

UNIVERSAL STANDARD DEFINITION: The magnification aid industry has not used a recognized, truly universal definition or method of measuring magnifying power that works with any type of simple or complex magnification device. Hughes has selected and herein proposes a standard definition which allows a fast and easy method of measuring quickly and on-the-spot the magnifying power (MP) of any visual magnification aid as a device.

HUGHES MAGNASCOPE: To work in conjunction with the standard definition of MP, Hughes has developed the "HUGHES MAGNASCOPE." This instrument's selection, calibration, and use is described in detail.

PROBLEM

Magnification aids have magnifying power values advertised, specified, and stamped on them, but it seems that almost everything but standard and zoom microscopes are incorrectly marked and do not conform to any recognized optical equation for determining magnifying power.

MAGNIFYING DEVICES SURVEY

We found that, after testing over 10 different 4X devices, almost all of them ran from 0.8X to 3X, and that 10X devices ran from 5.6X to 11X. Also three very complex, very expensive instruments were all about one-half their stated values. Because of these results, it is recommended that the inspection community should measure and certify all magnifying inspection devices in use and before placing any new ones in use.

Quick Hardware Solution At Hughes

Since the only devices that measured correctly had very small fields of view and poor resolution, Hughes designed and built special wide-angle, low distortion, high resolution, long-working distance, 4X and 10X magnifiers mounted in the center of fiber optics ring lights which can be hand held or mounted on a swivel-swing arm stand. Figures 1 and 2 show this inspection station.

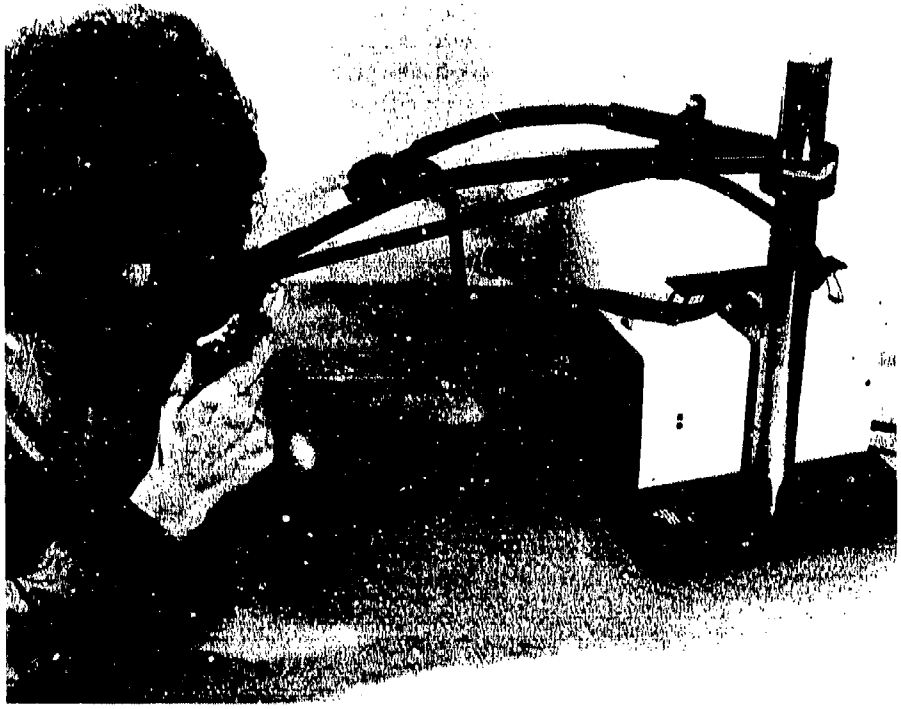

FIGURE 1. Hughes 4X/10X Swivel-Swing Arm or Handheld Magnifier with Fiber Optics Ring Light Inspection Station

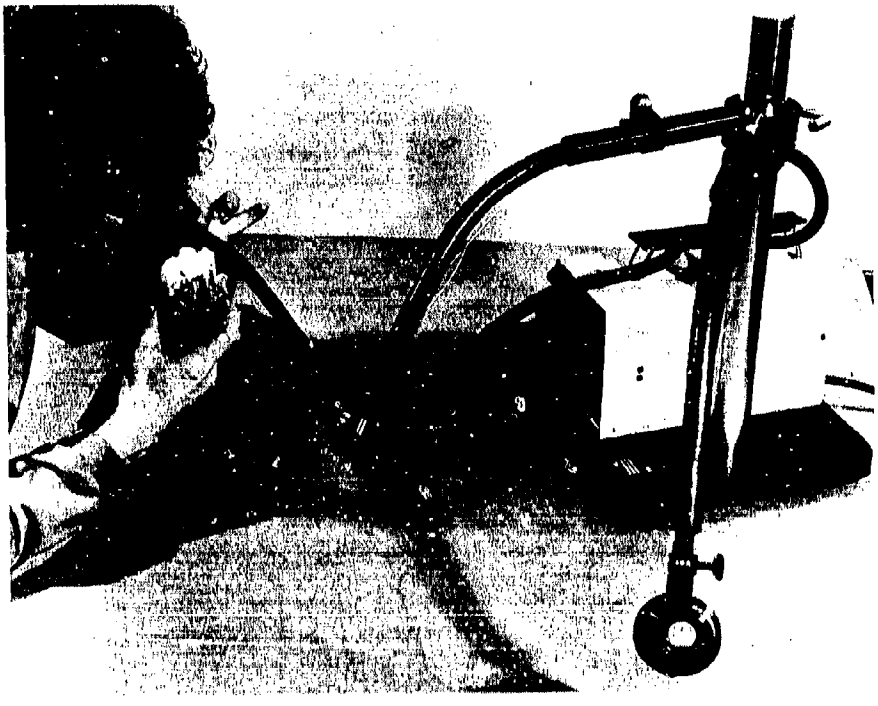

FIGURE 2. Hand Held Use of Hughes 4X/10X Magnifier with Ring Lighting

Advanced Instrument Solution

Hughes has also designed and is building a special "Optical Semiautomatic Inspection Station." This new system utilizes a stereo heads-up display with enhanced depth perception, very large pupils, long eye relief, wide field, high resolution, coplanar objects, optimized toe-in and eye focus distance, and computer driven reticle and focus. The object to be inspected is mounted on a computer driven X-Y table, and other concepts have been designed into the station to speed up operation and reduce operator fatigue. Figure 3 shows an illustration of this new inspection station.

FIGURE 3. HAC Tucson Optical Semiautomatic Inspection Station

UNIVERSAL DEFINITION NEED

The magnification aid industry has not used a recognized, truly universal equation, definition, or method of measuring magnifying power that works with all types of simple or complex magnification devices. Also, the more complex the magnifying device, the more difficult it is to measure real magnifying power. There are many equations and many ways to interpret their use. The more general equations use eye relief, lens spacings, and user's eye near or far focus conditions. The operator's contribution to system magnification is zero if his eye is focused at its far-point, infinity; however, if the operator's eye is focused at its near point of 10 inches, system magnification is one plus the magnifier aid's value. This leads to confusion about whether the magnifying power should be measured for the device or as system magnifying power that includes the operator's contribution to magnification.

Since it is desirable to define one standard method and since the condition of the operator's eye focus is not easily controllable or certifiable, its effects should be eliminated from definitions or measurements of magnifying power. Therefore, when defining magnifying power, the operator's eye should be defined as focused at infinity so it has no effect on measuring the magnifying power of the device. This can result in magnification device specifications that are measurable and certifiable.

In order to end confusion and give one standard definition with a simple method of using it, this paper proposes a single standard definition with relative tolerances and an example of a fast and easy method of measuring on-the-spot magnifying power (MP) of any type of visual aid device.

PROPOSED STANDARD DEFINITION FOR MAGNIFYING POWER (MP)

The apparent size of an object viewed with the eye is dependent upon the size of image formed inside the eye on the retina. This image size is directly related to the angle subtended by the object at the eye (see Figure 4).

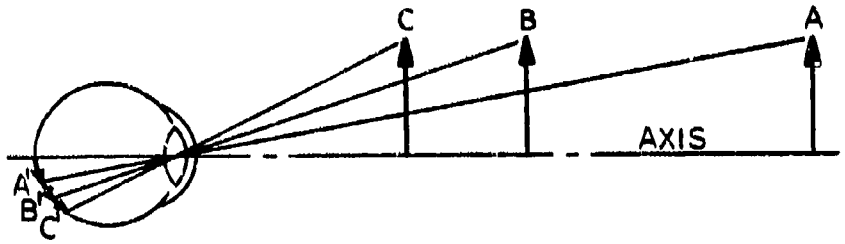

FIGURE 4. Image Size Increase vs Object Closeness

As an object is brought closer to the eye, it subtends a larger angle and forms a larger image on the retina. The eye, however, is limited in its ability to focus on near objects. The "average" observer cannot focus sharply on objects closer than 10 inches from the eye. This is referred to as the near point of the eye and defined as unity magnifying power.

If a magnifier (positive or convex lens) is placed in front of the eye, the effective near point is moved closer to the eye, thus increasing the subtended angle and therefore the size of the retinal image (see Figure 5). The size of this "magnified" image is compared to the size of the image when viewed at the near point with the unaided eye to give the "magnifying power" of the magnifier device.

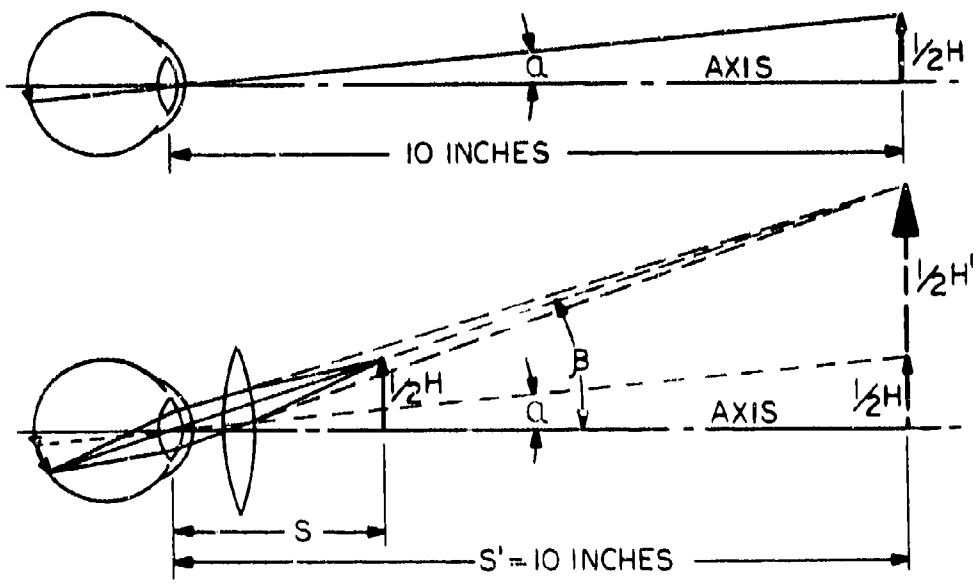

FIGURE 5. Image Size Increase with Magnifier Use

For example, if the image is two times the size of the image with the unaided eye viewed at 10 inches distance, the power is "2X."

The height of the retinal image is proportional to the tangent of the angle subtended and, in general, magnification or magnifying power is defined as the ratio of these retinal image heights.

The following is a proposed universal standard definition for magnifying power of any type of visual aid device. It was derived by combining equations and definitions from Section 7 of MIL-HDBK-141, MILITARY STANDARDIZATION HANDBOOK/OPTICAL DESIGN.

MAGNIFYING POWER (MP)

The magnifying power "MP" for a visual magnification aid/device shall be determined with the device focused so its image appears at infinity and by using the equation

$$MP = \frac{\text{Tangent } \beta}{\text{Tangent } \alpha} \qquad (1)$$

where ß shall be one-half the angle subtended by the image H' of an object H as seen through and centered in the field of view of the magnification aid/device, α shall be one-half the angle subtended by the object H as seen at 10 inches by the unaided eye, and Tangent α equals 1/2 H measured in inches divided by 10.

Figure 6 illustrates the relationship between ß, α, and H', and H.

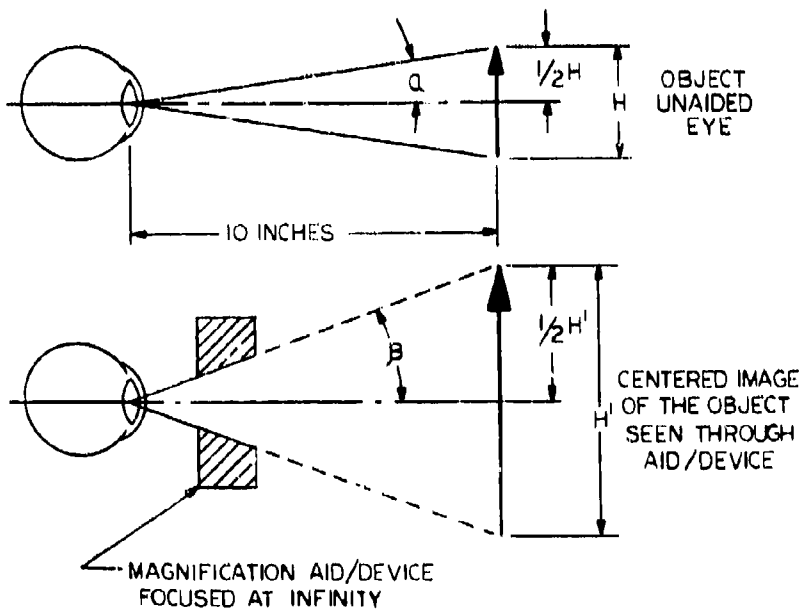

FIGURE 6.

With magnifying power (MP) defined, a functional, realistic MP tolerance should also be considered. This will allow manufacturers of magnifier devices, specification writers, and quality calibration activities to all work toward a common functional goal.

The following realistic functional tolerances are proposed:

1) Magnifiers with a MP of 4X to 25X should be manufactured such that MP is controlled to $\pm 10\%$.

2) Specifications that call out MP requirements that have to be measured and certified should specify the required MP with a tolerance of $\pm 15\%$. For example, "Solder joints shall be inspected with a device that produces a magnifying power of 10 $\pm 15\%$.

3) Calibration instrumentation and procedures used to measure MP of a magnifier shall be capable of accuracies better than $\pm 4\%$.

4) For magnifiers with an MP of less than 4.00, the above tolerances should be doubled.

MEASURING METHOD

This paper proposes a simple method that is fast to use once a reference angle measuring instrument is constructed and calibrated. The following describes how to choose this instrument, how to calibrate it, and how to use it to measure magnifying power of any visual aid used to add magnification to the naked eye.

For the rest of this discussion, this magnifying power measuring instrument shall be referred to as the "HUGHES Magnascope."

Basically, the "HUGHES Magnascope" is a telescope that is focused at infinity and that contains a calibrated 1/2 field angle reticle. When used to view through a magnifier device under test, an observer can make a reading of a measuring scale and perform a simple calculation to determine magnifying power. The "HUGHES Magnascope" may also be used in conjunction with specially calibrated "Object Target Scale" and measure magnifying power with a direct reading.

SELECTION OF MEASURING INSTRUMENT TO BE MADE INTO A "HUGHES MAGNASCOPE"

An instrument must be made or selected that can be calibrated and can be easily used to measure ß (the 1/2-angle subtended by the image of an object seen through the magnifier). Select a small low-power telescope with a symmetrical reticle target pattern that can be calibrated for a 1/2-field angle. The telescope eyepiece must be focusable to the reticle, and the telescope objective lens must be focused at infinity, or focusable to infinity so that the "HUGHES Magnascope" will be used to measure the magnifier's infinity-focused image. Also, the objective lens of the telescope must be capable of being apertured down to 4 to 5 mm diameter to simulate the eye's pupil size.

Telescopes of this type are called alignment telescopes, or autocollimators. A very compact, reasonably priced, and handy-to-use telescope that might be considered is the "#14 Walters 8 x 30 Monocular With Grid" that comes with a usable target reticle already focused at infinity.

S. Walters, Inc.
32208 Oakshore Drive
Westlake Village, CA 91361
Phone (818) 706-2202

CALIBRATION FOR TANGENT (ß MAGNASCOPE)

After selection of the telescope to be made into a "HUGHES Magnascope," standard optical instrumentation methods of autocollomating may be used to position the reticle at the infinity focus of the objective. If this is not convenient, a telescope already focused at infinity may be purchased.

Next, a 4 to 5 mm diameter aperture must be placed in front of the telescope's objective lens. This simulates the observer's eye pupil size when measuring magnifiers later and also reduces parallax errors when calibrating the "HUGHES Magnascope." If using the Walters monocular, the lens cap for the objective that comes with the monocular may be used by placing a hole in its center and placing it on the monocular.

With the telescope objective lens focused at infinity, the eyepiece shall be focused on its reticle while viewing a yardstick 2000 inches away from the objective lens of the telescope. Measure (1/2 H Magnascope) the distance subtended from the center of the reticle of the telescope to the mark chosen on the reticle pattern you want to calibrate for Tangent (ß Magnascope). An easy way to measure this distance is to use two light-colored pencils as markers for the yardstick that is placed against a dark-colored background. Place one pencil perpendicular to and at the start of the yardstick. Position the telescope so the center of its (ß Magnascope) reticle pattern is aligned with the pencil at the start of the yardstick. Then move the second pencil out along the yardstick until it is in alignment with the mark on the (ß Magnascope) reticle pattern to be calibrated. This distance is (1/2 H Magnascope) measured in inches. See Figure 7.

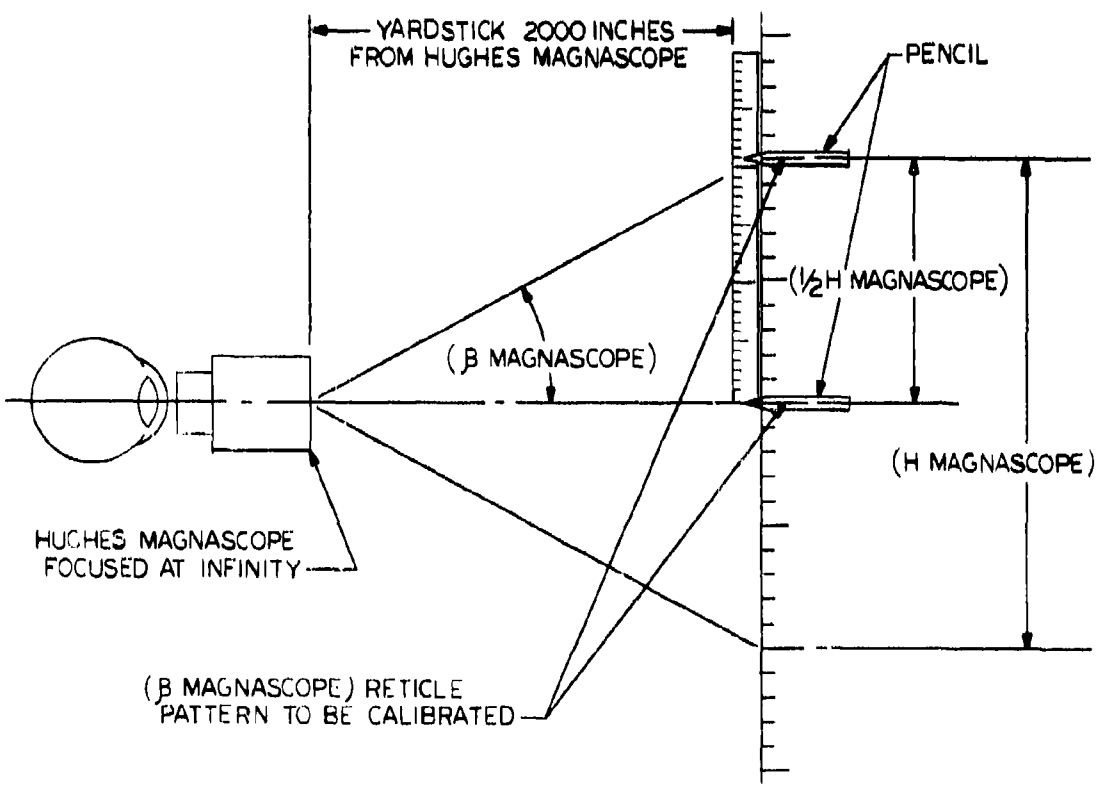

FIGURE 7.

If you are using the Walters 8 x 30 monocular for your "HUGHES Magnascope," measure the distance from the center of the reticle to the mark defined by #1 which defines the location of the tenth mark from the center (see Figure 8).

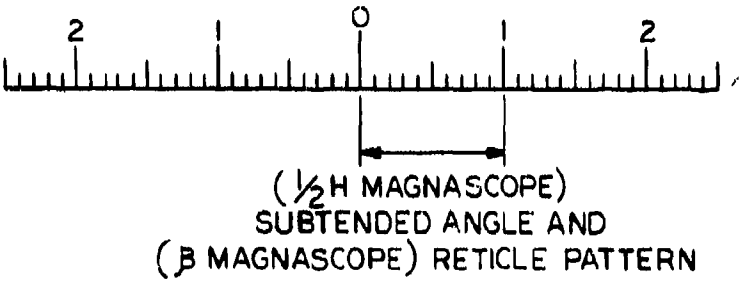

FIGURE 8. Walters Monocular Reticle

As a rough guide, the distance (1/2 H Magnascope) for the Walters monocular is about 25 inches. However, remember, because of manufacturing tolerance for reticles and for objective lens focal length of the monocular, each Walters monocular has to be calibrated individually for (1/2 H Magnascope). Values in this paper should only be used as reference examples.

Now that (1/2 H Magnascope) is known, Tangent (ß Magnascope) can be calculated using the following equation:

$$\text{Tangent (ß Magnascope)} = \frac{\text{(1/2 H Magnascope)}}{\text{Magnascope to Object Distance}} \tag{2}$$

$$\text{Tangent (ß Magnascope)} = \frac{\text{(1/2 H Magnascope) measured in inches}}{2000}$$

$$\text{i.e.: Tangent (ß Magnascope-Walters Monocular)} = \frac{25}{2000} = 0.0125$$

This finishes calibration of the "HUGHES Magnascope" for Tangent (ß Magnascope). Now the magnascope can be used to measure (1/2 H Magnifier) that is needed to calculate Tangent α used in calculating magnifying power of a magnifier device.

DETERMINING (TANGENT α) USING THE CALIBRATED "HUGHES MAGNASCOPE"

Recall from the definition of magnifying power, ß equals 1/2 the angle subtended by the image H' of the object H as seen through the magnifier and α equals 1/2 the angle subtended by the object H as seen at 10 inches by the unaided eye. Also recall

$$\text{Tangent } \alpha = \frac{\text{1/2 H measured in inches}}{10}$$

or

$$\text{Tangent } \alpha = \frac{\text{(1/2 H magnifier) measured in inches}}{10} \qquad (3)$$

where (1/2 H magnifier) is defined as the object size subtended by the (ß magnascope) reticle pattern when looking through a magnifier under test with the "HUGHES Magnascope."

To measure (1/2 H magnifier) the following steps should be performed:

1) The calibrated "HUGHES Magnascope" should have its eyepiece focused so that the reticle image is sharp. The 4 to 5 mm diameter aperture should be in front of the telescope's objective lens to simulate the observer's eye pupil size.

2) Using the magnification aid to be tested, a finely divided ruler or scale is observed and focused on with its edge in the center of the magnifier's field of view.

   Note: A 0.1 inch linear scale graticule with 100 divisions of 0.001 inch increments works well with the Walters Monocular. This scale is stocked as part number 11-8703 by Ealing, Pleasant Street, South Natick, MA 01760, phone (617) 655-7000 or by part number 70.0166 by Rolyn Optics Company, 738 Arrow Grand Circle, Covina, CA 91722-2199, phone (818) 915-5707.

3) The location of the user's eye relative to the magnifier aid in use should be noted. The "HUGHES" Magnascope's" objective lens should be located in the same relative location with respect to the magnifier aid as that which the eye was in while using the magnifier aid. It is desirable to use a holding fixture to keep the "HUGHES Magnascope" firmly positioned relative to the magnifier under test.

4) The Magnifier Aid and the "HUGHES Magnascope's" relative spacing must be fixed and focused on the scale by moving them as one, together, toward and away from the scale. Again, a holding fixture is desirable to accomplish this focus.

5) With the "HUGHES Magnascope's" reticle center aligned at the starting edge of the scale, measure (1/2 H Magnifier) the distance subtended on the scale by the (ß Magnascope) reticle pattern calibrated earlier.

When measuring a 10 power magnifier using the Walters monocular, the (ß Magnascope) reticle pattern calibrated was 10 units from center and that mark subtends a (1/2 H Magnifier) scale distance of approximately 0.0125 inches.

Now that (1/2 H Magnifier) is known, Tangent α can be determined from equation (3).

$$\text{Tangent } (\alpha \text{ Walters monocular}) = \frac{\text{(1/2 H Magnifier) measured in inches}}{10}$$

$$= \frac{0.0125}{10} = 0.00125$$

CALCULATION OF MAGNIFYING POWER

Now that Tangent (ß Magnascope), (1/2 H Magnifier), and Tangent α are known, magnifying power of the magnification aid can be calculated using equations 1 and 3.

$$MP = \frac{\text{Tangent ß}}{\text{Tangent } \alpha}$$

$$MP = \frac{\text{Tangent (ß Magnascope)}}{\frac{\text{(1/2 H Magnifier)}}{10}} \tag{4}$$

With the Walters monocular calibrated "HUGHES Magnascope" measuring a 10 power magnifier aid/device, MP calculates to be the following:

$$MP = \frac{\frac{25}{2000}}{\frac{0.0125}{10}}$$

$$MP = 10$$

Now that this calculation has been made to show how MP is calculated, and a "HUGHES Magnascope" has been made by calibrating the Walters monocular for Tangent (ß Magnascope), equation 4 for the calibrated instrument can be simplified as follows.

$$MP = \frac{\text{Tangent (ß Magnascope)}}{\frac{\text{(1/2 H Magnifier)}}{10}}$$

$$MP = \frac{10 \text{ x Tangent (ß Magnascope)}}{\text{(1/2 H Magnifier)}} \tag{5}$$

i.e.:

$$MP = \frac{10 \text{ x } \frac{25}{2000}}{\text{(1/2 H Magnifier)}}$$

$$MP = \frac{0.125}{\text{(1/2 H Magnifier)}} \tag{6}$$

Therefore, now that the "HUGHES Magnascope" Walters Monocular is calibrated to get magnifying power, all that is required is to divide the scale distance reading seen through any visual magnifier device that is defined by the collimated reticle marks into 0.125. Remember, each instrument must be calibrated and these are only reference values in the paper.

DIRECT READING MP MEASURING INSTRUMENT

A direct reading MP measuring "HUGHES Magnascope" can be made that requires no calculations. This can be done if a special reticle is designed and made for the "HUGHES Magnascope" to compliment a specially made "Object Target Scale" to be looked at through the Magnifier Aid.

A telescope similar to the #14 Walters 8 x 30 Monocular with Grid could again be used for the direct reading "HUGHES Magnascope."

If the #14 Walters monocular is used, its reticle has a center mark with 25 markings going out from each side of center. Define each unit of these 25 divisions as one power. This will allow measurement of up to 25 MP with this reticle. To use this reticle pattern, (1/2 H Magnascope) is measured for the reticle distance from the center to the 10 mark and Tangent (ß Magnascope) is calculated the same way as described in the Measuring Methods section of this paper.

Recall from equation 2 that Tangent (ß Magnascope) for the Walters monocular calibrated "HUGHES Magnascope" was the following:

$$\text{Tangent (ß Magnascope-Walters Monocular)} = \frac{25}{2000} = 0.0125$$

To define the spacings for construction of the special "Object Target Scale" that will be used for viewing at through the magnifier aid under test, equation 4 is used:

$$MP = \frac{\text{Tangent (ß Magnascope)}}{\frac{\text{(1/2 H Magnifier)}}{10}}$$

Now solving for (1/2 H Magnifier)

$$\text{(1/2 H Magnifier)} = \frac{10 \times \text{Tangent (ß Magnascope)}}{MP} \tag{7}$$

For the Walters monocular calibrated "HUGHES Magnascope" looking through a 10 power magnifier aid:

$$\text{(1/2 H Magnifier-Walters Monocular)} = \frac{10 \times \frac{25}{2000}}{10} = 0.0125 \tag{8}$$

Note: (1/2 H Magnifier-Walters Monocular) comes out to be the same "Object Target Scale" size for use with all MP values. Therefore, all that is necessary is to make one special "Object Target Scale" for use in measuring any device up to 25 MP when using the Walters Monocular. Figure 9 shows a typical "Object Target Scale."

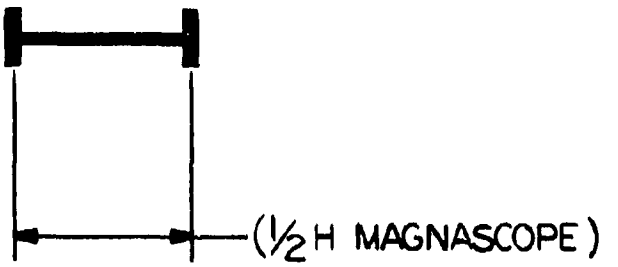

FIGURE 9. Direct Reading MP Special Object Target Scale

In use, the center of the "HUGHES Magnascope's" reticle is aligned with one edge mark on the special "Object Target Scale." Then the MP is read from the "HUGHES Magnascope" reticle's intersection with the opposite end mark of the "Object Target Scale."

Figure 10 shows what would be seen when measuring a 10X magnifier aid/device.

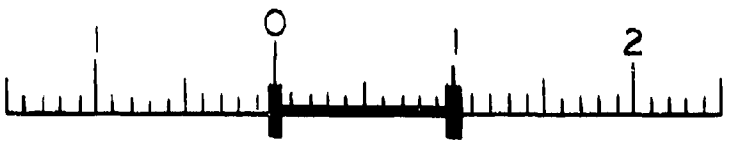

FIGURE 10. Direct Reading HUGHES Magnascope of a 10X Device

Figure 11 shows an added feature to further enhance the usefulness of the "Object Target Scale" by adding the ± 15% tolerance limits to one end.

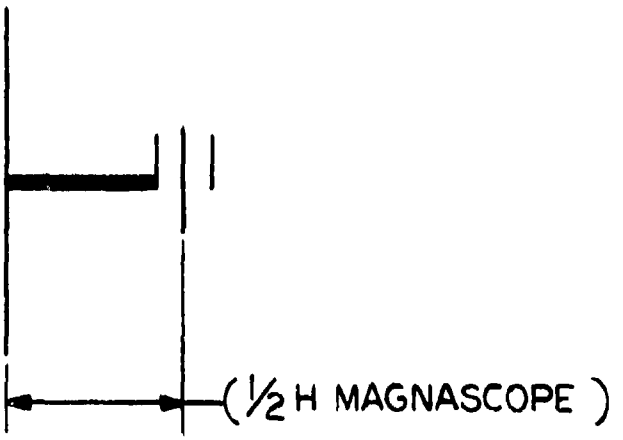

FIGURE 11. Improved Direct Reading MP Special Object Target Scale with ± 15% Tolerance Limits

Figure 12 shows what would be seen through the direct reading "HUGHES Magnascope" when looking through a 10X magnification aid/device at the tolerance limit "Object Target Scale."

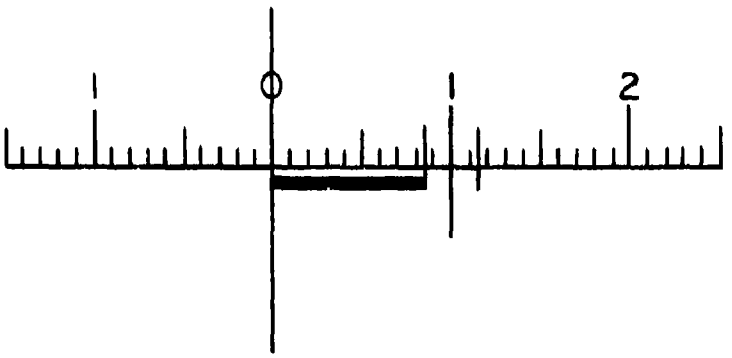

FIGURE 12. HUGHES Magnascope View Through a 10X Magnification Aid with ± 15% Tolerance Limits

Note: If more magnifying power reading accuracy is desired, the special "Object Target Scale" can be made four times larger or ten times larger. Then, when reading the "HUGHES Magnascope" Walters monocular reticle, each division will read 1/4 power with the four times larger "Object Target Scale" and will read 1/10 power per division with the ten times larger target.

Figure 13, 14, and 15 show the "HUGHES Magnascope" in use on a fluorescent ring light magnifier, a bench magnifier, and the HUGHES swivel 4X/10X Inspection Station.

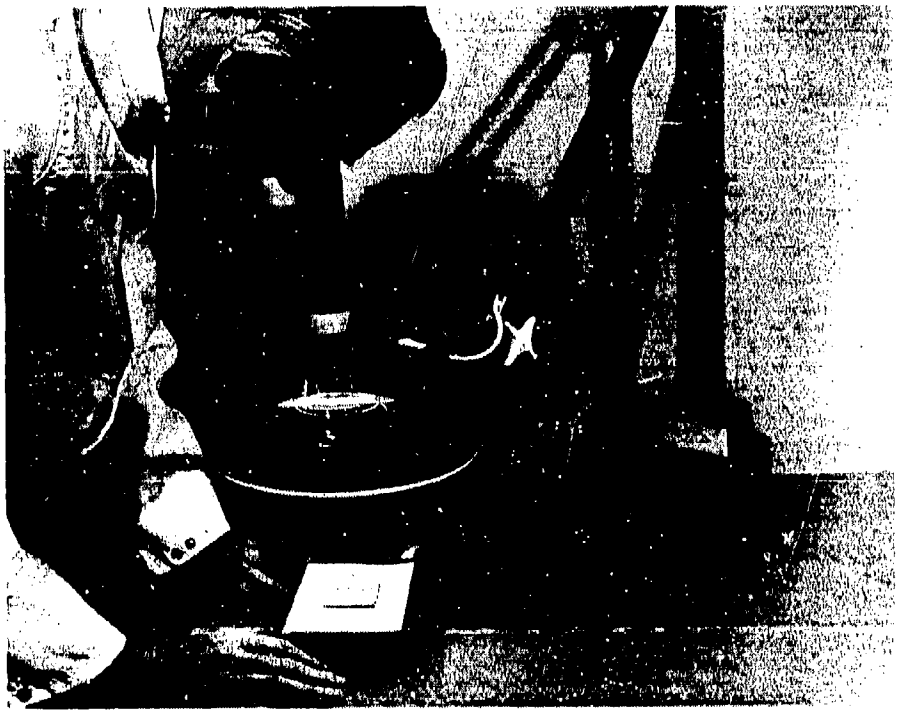

FIGURE 13. "HUGHES Magnascope" Testing A Flourescent Ring Light Magnifier

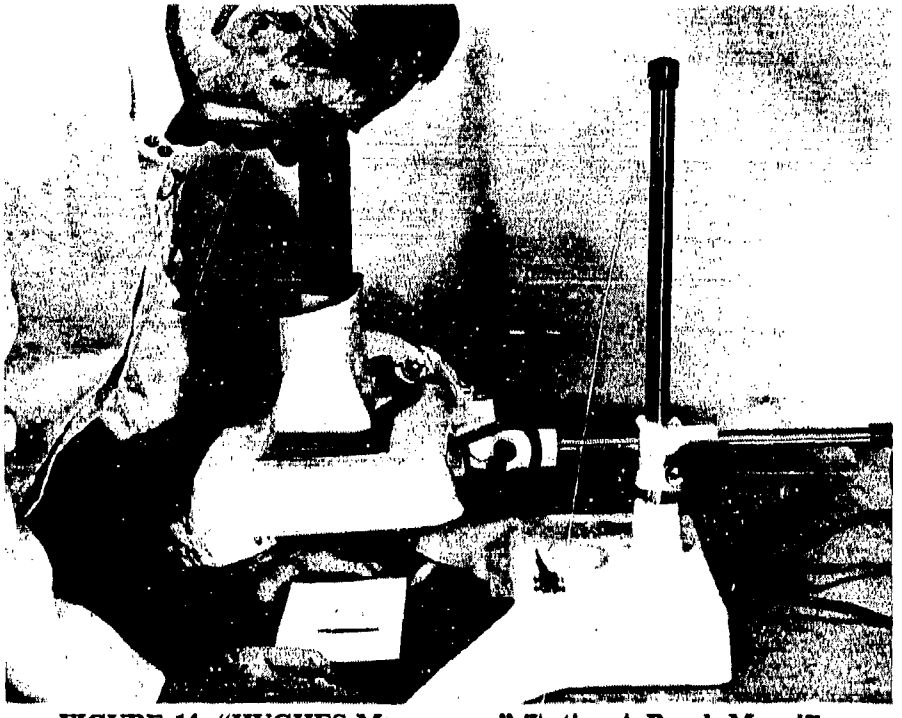

FIGURE 14. "HUGHES Magnascope" Testing A Bench Magnifier

FIGURE 15. "HUGHES Magnascope" Testing A Hughes 4X/10X Swivel-Arm Magnifier Station

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SURFACE MOUNTED DEVICES—FACTORS AFFECTING THE ADHESIVE PROPERTIES OF SYNTHETIC AND ROSIN-BASED SOLDER CREAMS

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Surface Mounted Devices.

Factors Affecting The Adhesive Properties Of Synthetic And Rosin-Based Solder Creams

Solder creams are mixtures of solder powder, flux, solvents and various other compounds blended in varying proportions to give the properties required for different end-uses. As with most products, the final result is a balance of properties, some being obtained at the expense of others.

In many creams, it has been apparent that good screen printing or dispensing characteristics have been obtained at the expense of tackiness. However, in many operations involving surface mount technology, no adhesive is used, the tackiness of the cream being the sole means of holding devices in place, in accurate alignment, between the assembly and the solder reflow areas.

To measure the adhesive properties of creams, a simple device has been developed from equipment available in most laboratories. This has been used to assess the effects of film thickness, solvent composition, rosin content, metal loading and other factors on device adhesion and other properties such as drying time. The interdependence of these factors has also been assessed to allow for better optimisation of the competing performance requirements.

Norman MacLeod, a Scotsman born in England, holds an honours degree in Organic Chemistry from the University of Nottingham. He has worked on a variety of subjects for the British Petroleum Company Research Centre, and has done extensive R&D in polymers for the Cookson Group. His work with the Research Department of Fry's Metals in London was on photosensitive coatings for printing plates, with an interest in flux chemistry and particularly the cleaning of flux residues. His work with Federated-Fry Metals has him commuting between the USA and England.

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Larry Hoover was graduated from the Williamsport Area Community College with an associate degree in Electrical Technology. He attended the University of Pittsburgh studying Electrical Engineering while employed by Bethlehem Steel and later U.S. Steel. Since 1982 he has been Department Head and Technical Representative for the manufacture of solder powders and flux.

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AUTOMATED INSPECTION OF SURFACE MOUNTED SOLDER CONNECTIONS A STATUS REPORT ON A FIRST INSTALLATION

by
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ABSTRACT

The acceptance of surface mounting in the electronics industry has been slowed by problems with component availability, electrical testing, and inspection. Industry suppliers and users have been working to solve these problems, and these problems are easing. Component manufacturers are offering substantially more devices in surface mountable packages. Automated test equipment vendors are offering test fixtures for surface mount circuit boards. And just recently, solder connection inspection has been automated through a "partnership" effort with a major electronics manufacturer. The result achieved in this successful first installation is the subject of this paper.

THE NEED FOR SOLDER QUALITY INSPECTION

Surface mounted devices are held in place on the circuit board by their solder connections. The same situation occurs on plated-thru-hole circuit boards. However, with surface mounting, there is no solder plug surrounding a pin thru a hole in the circuit board to give the connection added strength. Instead, the solder alone bonds the device to the circuit board, as shown in Exhibit 1. The electrical integrity of the circuit board is totally dependent upon the structural integrity of the solder connection. This issue of structural integrity, plus the large numbers of solder connections on each circuit board, are the impetus for automating solder connection inspection.

Surface mounting makes more electronic products man-portable or mobile in vehicles. With this portability or vehicular mobility comes shock, vibration, and extremes of temperature. Shock, vibration, and temperature approach or exceed levels that were previously associated only with military electronics. These higher stress levels must be sustained by the smaller solder connections characteristic of surface mounting. Numerous experts have cited how surface mounted solder connections are disposed to fatigue and creep failure.

STRESS AND ELECTRICAL TESTING

The structural integrity of solder connections can be assessed to some degree with "shake and bake" stress testing. However, this type of testing confronts the risk of wearing out the product before it ever reaches the customer. Further, the electrical testing that is used with "shake and bake", as well as that usually performed in regular manufacturing quality assurance, detects only the "open" or "short" conditions. Stress testing typically does not expose the structurally marginal connections that still conduct, but are long term candidates for failure, such as:

- o insufficient solder;
- o poor wetting;
- o excess solder or lead projection;
- o device or lead off position;
- o unwanted solder balls or splashes;
- o device tilted relative to the board;
- o porosity in the solder connection.

VISUAL INSPECTION

Visual inspection can detect gross defects, such as missing devices, bridges outside the devices, the absence of solder fillets, and non-wetting. However, visual inspection is qualitative rather than quantitative---it does not measure the extent to which a defect exists. Also, visual inspection relies upon the external appearance of the solder connection to infer its internal structural integrity. And with surface mounting, the solder connections are partially or fully underneath the devices, making visual inspection impractical.

STRUCTURAL INSPECTION

Structural inspection is not a new problem. For years, aerospace and casting manufacturers have used X-ray inspection to examine the structural integrity of castings for airframes, engines, and transmissions. Since solder connections are a "casting" formed by the surface tension of the molten solder and the surfaces of the device and the circuit board, X-ray techniques will work for solder connections. The keys to making X-ray techniques viable for solder connection inspection are to:

1) speed up the X-ray imaging process,
2) radiation from damaging electronic components,
3) improve X-ray imaging to resolve 0.001 inch features,
3) automate inspection to achieve fast, accurate results, and
4) make the techniques usable in the production line.

DEVELOPING A SOLDER QUALITY INSPECTION MACHINE

In 1984, we became aware of the need for structural inspection of solder connections in surface mounted electronics thru a customer, and developed the machine shown in Exhibit 2 specifically for solder connection inspection. This machine took "flash" X-ray images of each device on the circuit board to keep radiation from damaging the device, and automatically inspected the "structure" of each solder connection according to a "rule set" that took into consideration:

- o the type of device (PLCC, SOT, LCC, etc.);
- o the shape of the pad on the circuit board;
- o the amount of misalignment allowed between the device and the circuit board;
- o the range of solder connection thickness allowed;
- o the range of solder connection shape allowed;
- o the amount of porosity allowed.

This first machine administered a maximum dose of 5 RAD(Si) to each circuit board, was designed to "see" features as small as 0.002 inch in size, and used images like the one shown in Exhibit 3 to inspect each solder connection. A schematic for this first machine is shown in Exhibit 4. In operation, the machine used an electrical X-ray source to project a collimated beam of X-rays up through a 1" by 1" area of the circuit board. The X-ray shadow image of the solder connections was projected onto a fluorescent screen just above the circuit board. This screen converted the X-ray image into a visible light image, which was viewed by a high resolution video camera through a first surface mirror to keep the camera and optics out of the X-ray beam. The video image of the solder connections was input to a digital image processor, that performed the actual inspection under the direction of a set of programs in an IBM Personal Computer.

RESULTS ACHIEVED WITH THE FIRST MACHINE

In mid-1985, this first machine was installed in a surface mount production line to inspect 1000 circuit boards per day with J-leaded surface mounted ICs. Each circuit board had 252 solder connections, and inspection time per circuit board was 30 seconds. Since the customer's production line operated seven days per week, this first machine and its software have inspected more than 200,000 circuit boards. This large production volume has forced us to make our inspection programs effective for the wide variations found in production solder connections made with vapor phase reflow.

The defects identified by this first machine have been:

- o void (absence of solder joining lead to pad);
- o insufficient solder (including porosity);

- o bent lead (off position from pad);
- o leads touching (producing a short without a bridge);
- o solder bridge;
- o device off position (skewed or shifted);
- o device missing from board.

These defects are identified accurately and repeatably, and our customer is pleased with the performance of the machine (particularly since it has already paid for itself). However, there are some caveats on inspection accuracies.

Solder bridges and missing devices are practically always found, since they represent extreme conditions. Insufficients, bent leads, voids, and off positions are questions of the degree to which the defect is present. Through manual re-screening of automatically inspected circuit boards, we have learned that these defects are found roughly 95% to 99% of the time. The range from 95% to 99% is largely attributable to the variability of the human inspectors used to perform the re-screening. Inspectors do make "bad" calls on occasion. A more important facet is the relationship we found between increased defect detection and increased "false rejects", product rejected as bad when it is truly good.

THE IMPORTANCE OF ACCEPT/REJECT THRESHHOLDS

Exhibit 5 shows two overlapping distributions that help explain this relationship. The horizontal axis is a "measure of quality" that is a composite of many measurements of the size and thickness of each solder connection. The vertical axis is the number of solder connections with that measure of quality in a batch of boards. The accept/reject threshhold determines whether a solder connection is accepted as good or rejected as bad. Solder connections to the left of the threshhold are rejected as bad. Solder connections to the right of the threshhold are accepted as good.

This relationship between defect detection and false rejects can be seen in Exhibit 5. As the accept/reject threshhold is moved to the right, more and more defects are detected until practically none escape inspection. However, as defect detection grows in effectiveness, so does the number of good connections (the left "tail" of the "good" distribution) that will be falsely rejected as defective. This results from the overlap of the "good" and "bad" solder connection distributions, and reflects reality. We have found that the characteristics of marginally good solder connections significantly overlap those of marginally bad solder connections.

As a result of the relationship between the accept/reject threshholds and the economics of our customer, the accept/reject threshholds for the first machine have been set up to detect roughly

97% of all defects while making fewer than 5% false rejects. These performance levels are far better than those achievable with inspection personnel. Note that inspection by our machine is done before electrical testing to increase the effectiveness of electrical tests. For other customers with a different manufacturing process, and different costs for inspection, rework, scrap, and escape of defects, different accept/reject threshholds would be necessary to achieve the best economic return for their circumstances.

THE "STRUCTURAL" SOLDER QUALITY STANDARDS PROBLEM

As an aside comment, the requirement for flexible accept/reject threshholds, when coupled with the wide variations found in production solder connections, and the absence of complete information about what a good solder connection "looked like", almost prevented us from delivering a satisfactory working machine. Fortunately, our customer was willing to spend considerable time and money developing their own structural standards for what made solder connections good versus bad. This required stress cycling hundreds of circuit boards, analyzing each failure to establish causes, and then proceeding with production while monitoring production items for in-the-field failures on an on-going basis. All this work entailed considerable investment, and resulted in standards that are not consistent with present visual inspection standards. When structural standards are developed for other products, such as avionics, we feel these standards will not agree with existing visual inspection standards. Since a substantial beneficiary of these new structural standards would be the military, funding for standards development should be allocated as soon as possible, particularly in view of the increasing concerns over the structural viability of leadless surface mounted devices. Based on the experience of our customer, where practically no field failures now occur, these new standards would clearly help reduce in-service failures. And, our customer's product environment is 3+ G's of shock and vibration, ambient temperature from -40 F to +125 F, and humidity from 0% to 100%.

CONCLUSION

In concluding, it is difficult to extrapolate general savings rules from a single installation. However, we have shown with our first installation that automated X-ray inspection can dramatically reduce:

- the costs of inspection,
- the incidence of unnecessary rework on good boards,
- the recycling of boards thru rework as additional defects are cited,
- the costs of scrap by minimizing rework,
- the escape of defective boards

- the incidence of defects.

This last point is an often overlooked major benefit area. With the quantitative quality data that is a by-product of automated X-ray inspection, you can control your manufacturing process to make better product. Our first machine was installed in a new manufacturing line with completely new equipment. During process start-up, it was discovered that our machine could help set up the solder paste screen printer and reduce the incidence of voids, bridges and insufficients. During production, our machine continues to monitor paste printer performance by noting the incidence of bridges and insufficients. When our on-line defect reports show an increase in bridges or insufficients, the customer's personnel know how to adjust the process back into control. As a result, our customer has been able to achieve a significant increase in yield.

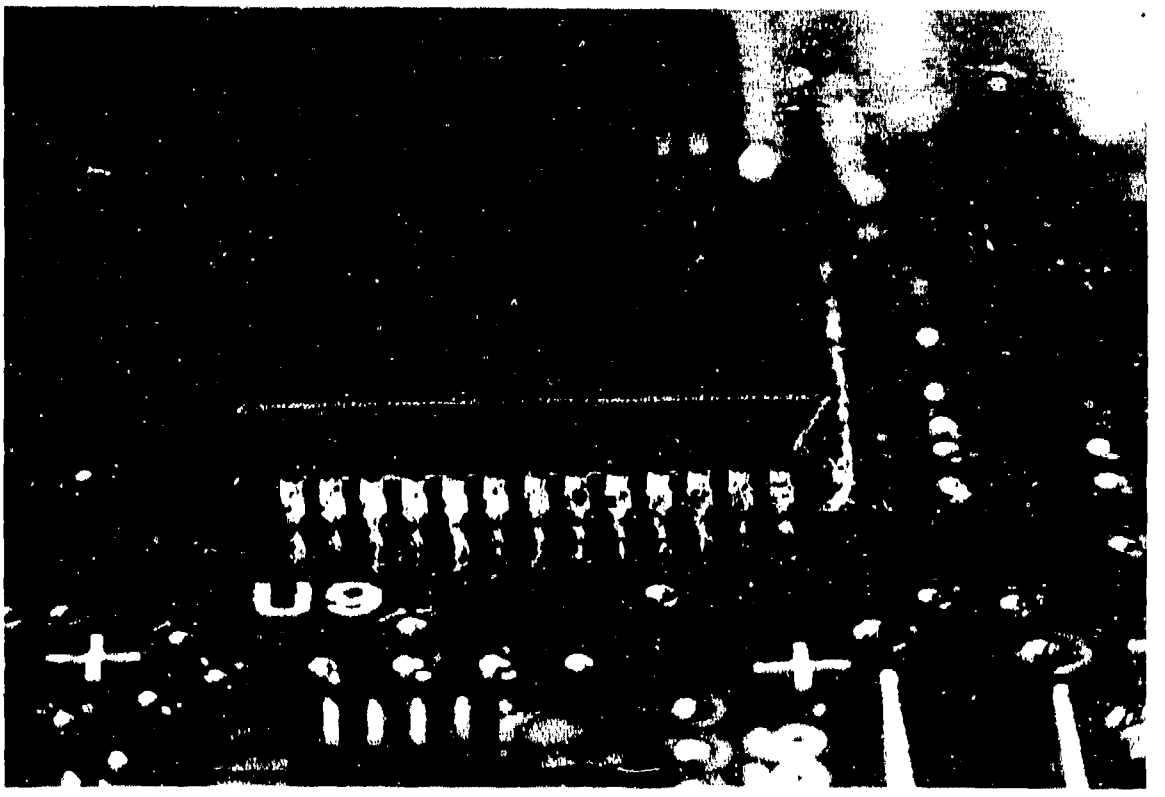

EXHIBIT 1 VISUAL IMAGE OF PLCC ON A CIRCUIT BOARD.

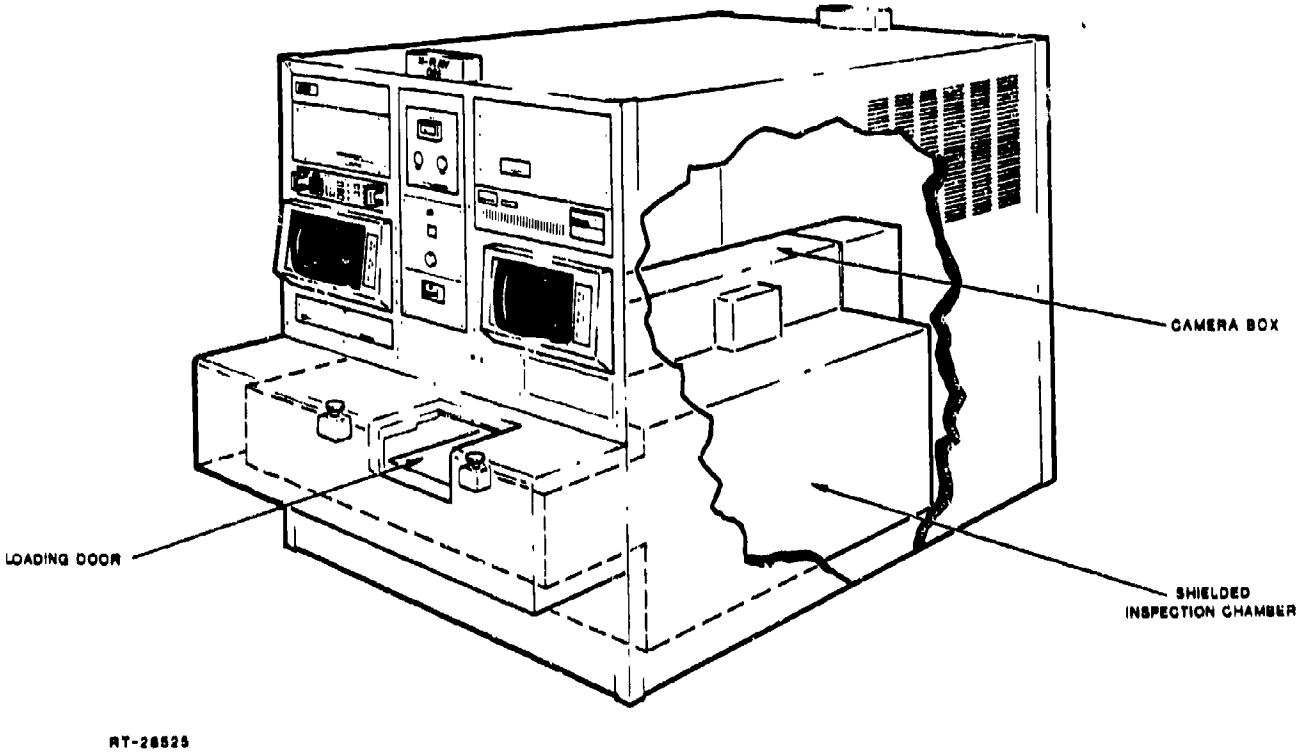

EXHIBIT 2 LINE DRAWING OF FIRST INSPECTION MACHINE.

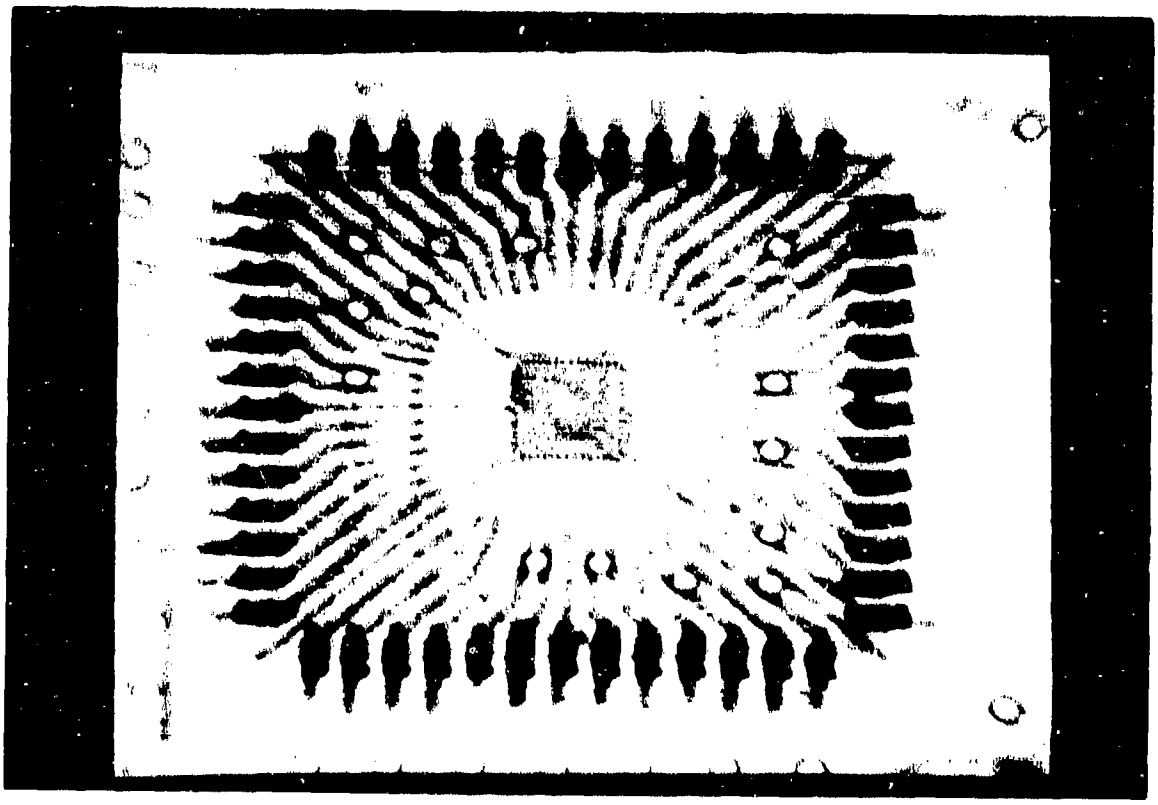

EXHIBIT 3 X-RAY IMAGE OF PLCC.

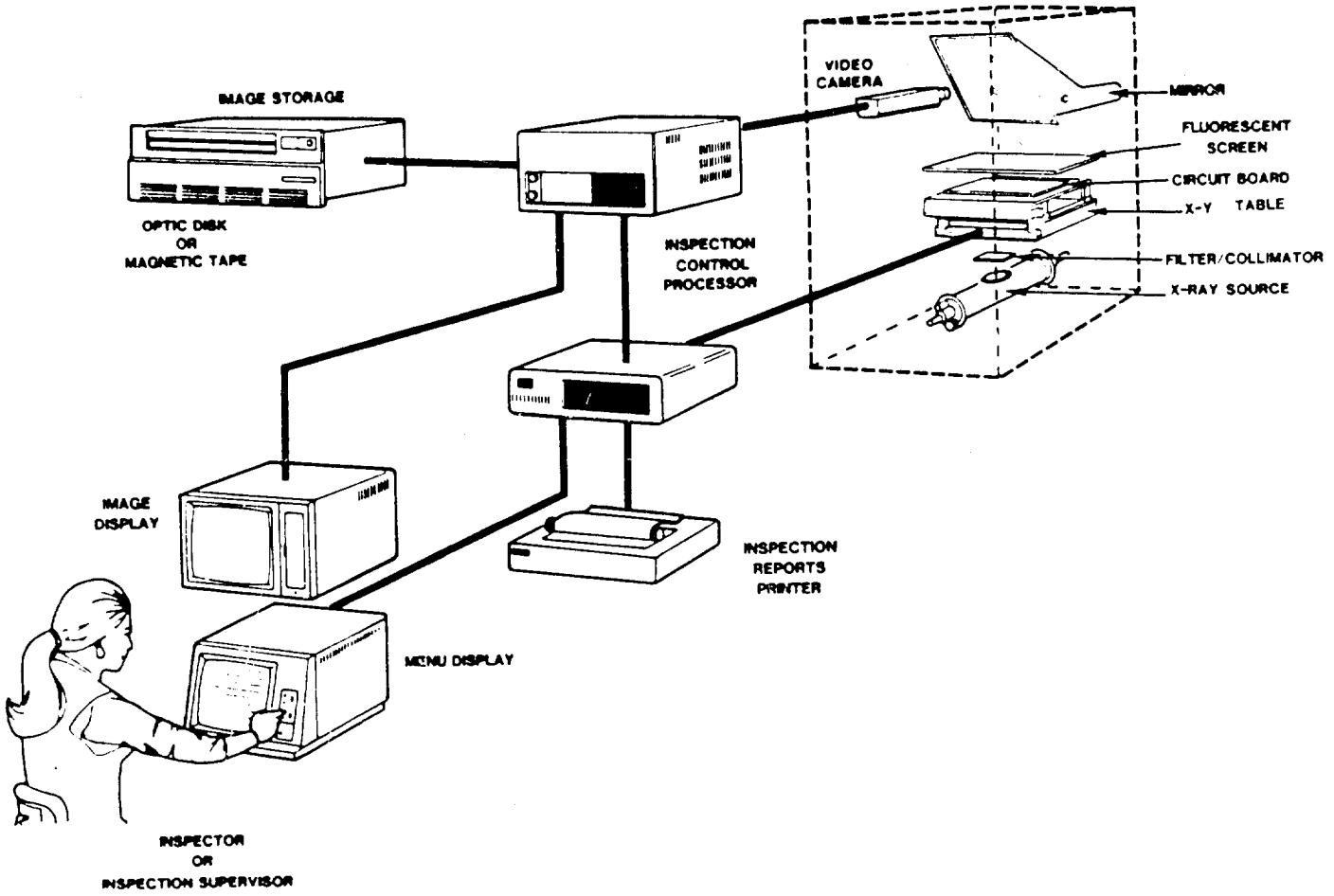

EXHIBIT 4 SCHEMATIC FOR FIRST INSPECTION MACHINE.

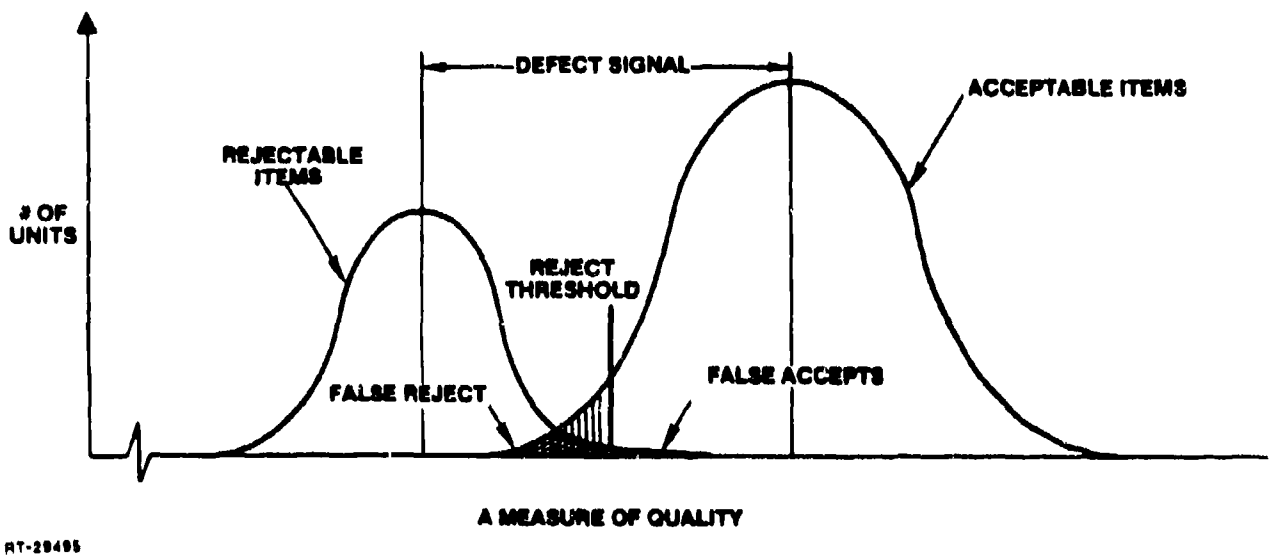

EXHIBIT 5 DISTRIBUTIONS SHOWING SOLDER CONNECTION QUALITY.

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SURFACE MOUNTED TECHNOLOGY ISSUES AND ANSWERS

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SOLDERABILITY OF CAPACITOR LEAD WIRES

by

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ABSTRACT

Solder-coated wire materials and capacitor lead wires have been studied using a wetting balance and examination of surface coverage after hot dipping. Effects of solder coating thickness, composition and microstructure, and of core metal composition were examined, as well as the effects of capacitor fabrication, burn-in testing, and steam aging. For the materials examined, the principal factor affecting wetting speed is the microstructure of the solder coating. Wires having coarse-structured coatings wet relatively slowly and are degraded by steam aging. Wires plated with a fine-structured coating by GTE Products Corporation wet very rapidly and are unaffected by steam aging. Lead wires hot-dipped after fabrication show intermediate wetting times which increase rapidly with steam aging. For components which utilize fabrication processes which do not modify the structure of the lead-wire coatings, such as hermetically sealed tantalum and film capacitors, optimum solderability is achieved using wire having fine-grained electroplated, or reflowed, coatings.

INTRODUCTION

Solderability of electronic components has received increased emphasis recently. To try to assure acceptable lead-wire solderability, component users are considering requirements more demanding than the present version of TM 208 of MIL-STD 202, such as wetting balance (meniscograph) tests similar to TM 2022 of MIL-STD 883-C and an increased steam aging duration before testing. Some users are specifying processing requirements, such as hot dipping of leads following fabrication and testing, in addition to performance requirements.

Leads on Kemet capacitors made by Union Carbide Corporation are made using wire of several different core materials coated with 7.6 to 12.7 μm (300 to 500 μin.) of solder. These wires, which include copper, nickel, copper-clad steel (CCS), nickel-clad steel (NCS), and nickel-clad copper (NCC), are purchased from a number of vendors. In order to assess the quality of these lead-wire materials, a program was undertaken to characterize their solderability using a wetting balance and surface coverage inspection. Lead wires on finished parts were examined along with incoming wire to determine the effects of fabrication and testing, and steam aging was used to simulate extended storage. Techniques for measuring the composition, thickness, and microstructure of solder coatings on wires were also evaluated so that these parameters, as well as base metal composition and intermetallic layer thickness could be related to solderability.

CHARACTERIZATION OF SOLDER COATINGS

COMPOSITION

Several different methods were used to measure the composition of solder coatings on wires.

Wet Chemical Techniques

Two methods of composition measurement which involve dissolving wire samples in acid followed by analysis of the acid solution were used to determine the concentrations of lead, tin, and elements present in the wire core. Methods used to analyze the solution were

(1) induction coupled plasma (ICP)

(2) atomic absorption (AA)

X-Ray Techniques

Three X-ray methods were used to measure solder composition:

(1) a Philips "XRF" X-ray fluorescence spectrometer,

(2) a Seiko SFT 157 XRF coating analyzer,

(3) a Tracor Northern TN5500 energy-dispersive X-ray spectrometer connected to an ETEC scanning electron microscope.

Differential Scanning Colorimeter (DSC) Technique

A technique described by R. L. Fryans (Reference 1) requiring measurement of heat of fusion on solder removed from a wire was carried out on a Perkin-Elmer DSC-2 in our laboratory by T. Su.

Coating composition measurements on the eight different wire materials given in Table I were measured by each of the above techniques. A plot of the weight percent tin measured for each sample is shown in Figure 1, using the ICP wet chemical method as the standard for comparison. The other wet chemical technique (AA) agrees well with ICP. The X-ray techniques give tin concentrations lower than the wet chemical methods. The Seiko SFT 157 is closest, giving results consistently 3 to 4% too low. The EDS method gives very scattered results, generally much lower than the other techniques. Segregation of lead to the free surface of the solder (Reference 2) may be the cause of the low tin measurements obtained using X-ray techniques. The DSC method is generally in good agreement with ICP.

THICKNESS

Four techniques for measuring solder coating thickness were evaluated.

Wet Chemical

Determination of the relative concentrations of lead/tin and core metals for a wire sample allows the coating thickness to be calculated. The techniques used for composition measurements (ICP and AA) were also used to determine coating thickness.

X-Ray Fluorescence

The Seiko XFT 157, which is designed to measure coating thickness by X-ray absorption, was used following calibration with standards of known thickness.

Microscope Examination

Scanning electron microscope examination of cross-sectioned and polished wire specimens was used to

TABLE 1. Solder Coating Properties on Eight Wire Materials as Measured by Different Techniques

Wire	Composition, Wt.% Sn						Thickness, μm				Mean Intercept Distance, μm
	Wet Chemical			Seiko	Philips	TN5500 EDS	Wet Chemical		Seiko	Cross-	
	ICP	AA	DSC	SFT 157	XRF	(SEM)	ICP	AA	SFT 157	section	Heyn Method
Electroplated 60/40 on Ni	61.5	64.5	63.7	57	49	58	7.9	8.6	9.7	8.8	0.5
Reflowed 60/40 on Ni	59.7	-	64.4	55	48	46	7.7	-	9.0	6.0	2.5
Electroplated 60/40 on CCS	59.5	60.5	63.6	56	51	44	10.4	11.2	10.5	6.6	3.5
Electroplated 60/40 on CCS	58.1	58.8	65.7	55	54	46	7.6	8.0	8.1	4.3/5.2	4.0
Electroplated 60/40 on Cu	64.0	-	64.9	60	49	29	7.9	-	8.3	8.8	3.5
Reflowed 30/70 on CCS	34.9	33.8	29.4	31	25	22	7.1	7.6	8.0	4.5/8.4	3.0
Electroplated 60/40 on CCS	57.8	-	57.3	53	54	36	8.8	-	9.4	8.3/12.4	3.0
Electroplated 60/40 on Ni	60.3	-	63.6	58	51	54	8.9	-	9.9	7.5	4.5

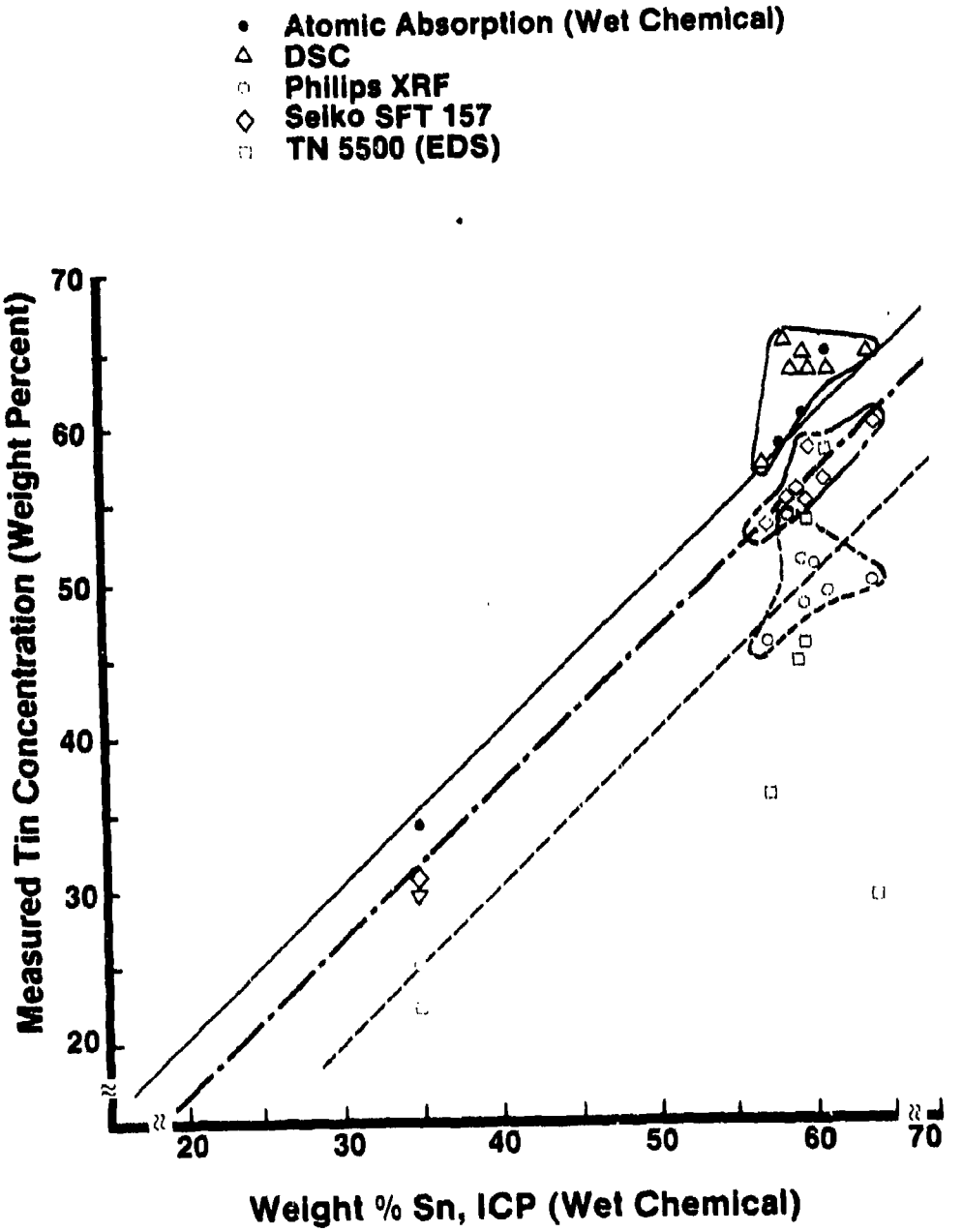


FIGURE 1. Tin Concentration of Solder Coatings on Wire Samples Measured by Different Techniques vs. Thickness Measured by ICP.

directly measure coating thickness, generally on 2000X backscattered electron images.

Coating thickness measurements on the same eight materials used in the composition study (Table I) are graphed in Figure 2, again using ICP measurements as the standard of comparison. The Seiko SFT 157 and atomic absorption measurements are 0.5 to 1.5 µm (20 t0 60 µin) higher. Cross sectional measurements are very scattered, prcbably due to problems with smearing and edge retention during mounting and polishing. Improved metallographic procedures have reduced the scatter since these data were collected, but cross-section measurement is still considered less accurate than the other methods.

The above results show that the Seiko SFT 157 provides coating thickness and composition measurements in close agreement with the more time-consuming wet chemical methods. Because of its speed and convenience, the Seiko instrument has been chosen for routine characterization of solder coatings on wire materials.

MICROSTRUCTURE

The microstructure of solder coatings was characterized using SEM backscattered electron images, on which lead-rich phases appear light and tin-rich phases appear dark. The average size of individual tin-and-lead-rich regions in the solders was approximated using a lineal intercept procedure, similar to the Heyn method used to determine the grain size of materials (Reference 3). The average intercept distance between tin-lead phase boundaries is measured by counting the number of phase boundary intersections on a line of known length.

SOLDERABILITY TESTING

Solderability of wire materials and capacitor leads was measured using TM 208 of MIL-STD 202 with variable steam aging times, and by a wetting balance. The wetting balance used is a Multicore Universal Solderability Tester interfaced to a Hewlett Packard 85B computer through an H-P 3478A multimeter. The system automatically measures and stores wetting force approximately 70 times per second beginning with electrical contact between the wire sample and the solder bath. The instrument settings used in this study are given below.

Balance Range:	0.75 g
Immersion Speed:	20 mm/s

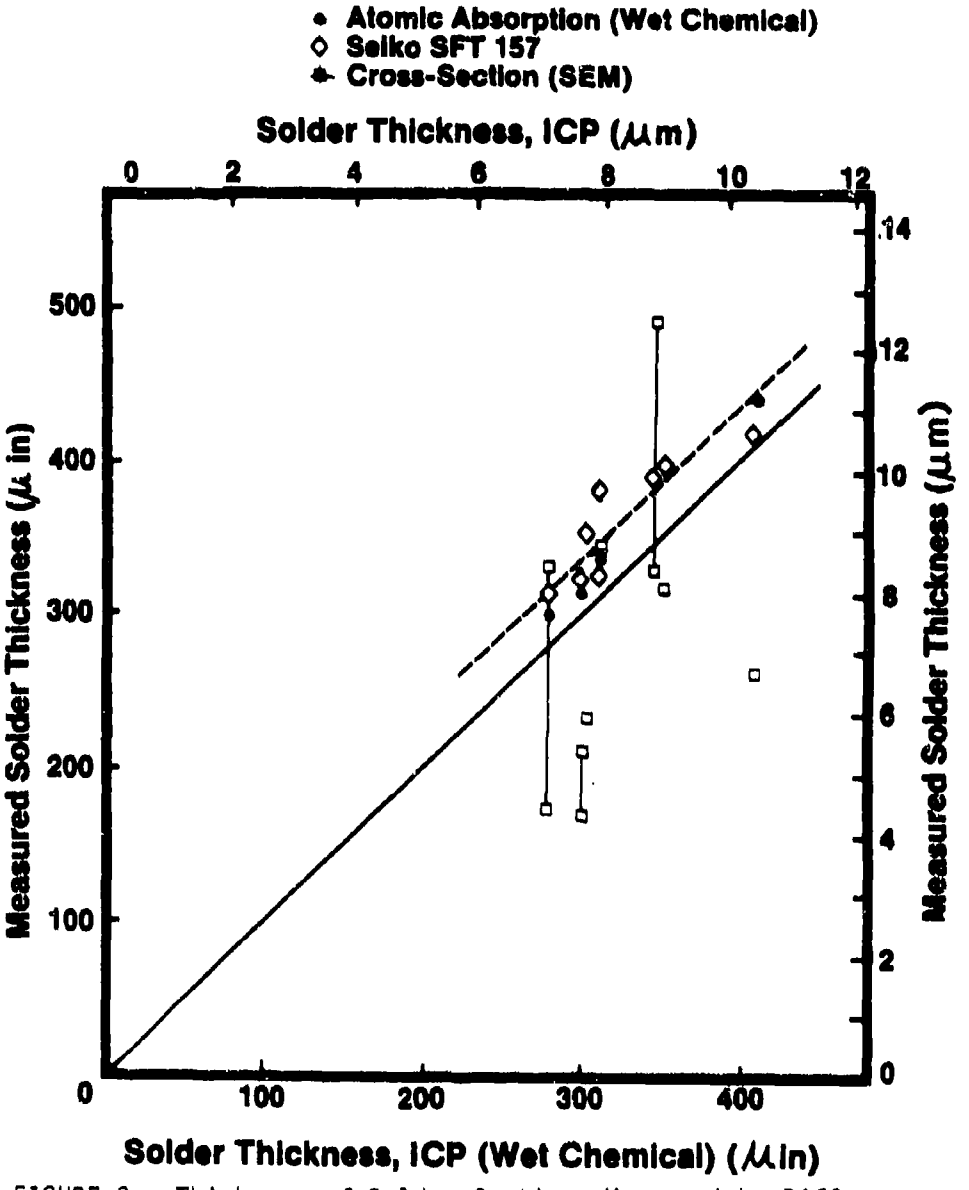


FIGURE 2. Thickness of Solder Coatings Measured by Different Techniques vs. Thickness Measured by ICP. Vertical Lines Connect Replicate Cross-Section Measurements on One Material.

Depth:	2.5 mm
Duration:	5 s
Temperature:	245 deg.C
Solder Alloy:	60 Sn-40 Pb
Flux:	Type R (Alpha 100)

After completion of a test, a graph of wetting force vs. time is drawn and parameters, such as time to reach zero force, maximum wetting force (corrected for buoyancy), and time to reach 0.67 maximum wetting force, are determined and printed out. Five specimens of each wire sample were generally tested to characterize it.

Test method 2022 of MIL-STD 883-C specifies that the time to reach zero force be less than 0.6 second and that the time to reach 0.67 maximum force be less than 1 second. Nearly all of the samples tested satisfy the zero force time requirement. A much smaller faction satisfied the 0.67 maximum force requirement. The time to reach 0.67 maximum wetting force was found to be the wetting-balance parameter most sensitive to differences in wire materials and is used as the principal solderability parameter in this paper.

The effects of core-metal composition and solder composition, thickness, and microstructure on solderability were examined for incoming wires. Samples of various wires were also studied after exposure to burn-in test thermal cycles (85 deg.C for 40 hours for tantalum capacitors, 125 deg.C for 100 hours for ceramic and film capacitors) which produce an intermetallic layer at the solder-core interface, and after steam aging at approximately 100 deg.C, 100% relative humidity for various times.

SOLDER COATING PROPERTIES

Within the range of coating thickness examined (7.1 to 10.9 µm (280 to 430 µin.)) no effect of thickness on solderability was found. Solder composition, which varied from 30 to 64% tin, also did not show a systematic effect on solderability. Major differences in solderability, however, were seen for solders having different microstructures. Two general types of electroplated solder coatings were found: fine structured solders (mean intercept distance $\tilde{=}$0.5µm (20 µin.)) plated on some wires by GTE Products Corporation and coarse-structured solders (mean intercept distance of 3 to 4.5 µm (120 to 175 µin.)) found on all other electroplated wires. Examples of these coatings for 60 Sn-40 Pb and 30 Sn-70 Pb solders are illustrated in Figure 3. Wires with fine-grained coatings exhibit very rapid wetting ($t_{0.67MF}$

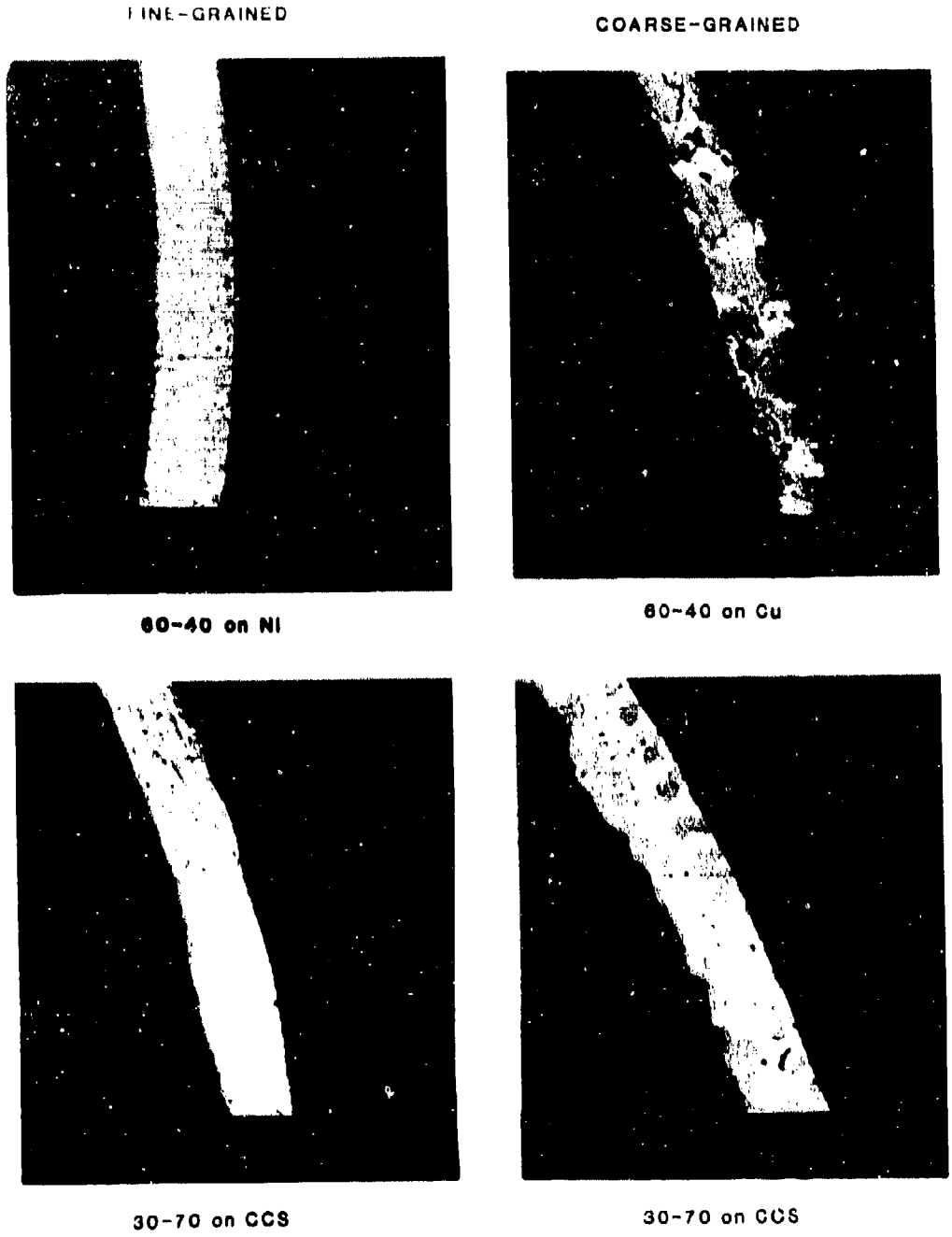


FIGURE 3. Backscattered Electron Images of Polished Cross Sections of Solder-Coated Wires. Lead-Rich Phase Appears Light, Tin-Rich Phase Dark

≅0.5 sec) as illustrated in the wetting curves shown in Figure 4. The wetting curves for these wires are not significantly changed by burn-in testing or steam aging up to 24 hours. Some of the fine-grained solder-coated wires show a decrease in wetting force after achieving a maximum value, as seen in the copper-clad steel specimen in Figure 4. The cause of this and its effect on solder-joint quality are not known. Complete solder coverage is always seen after hot dipping on these wires, with no visible dewetting.

Wires coated with coarse-grained solder generally require longer times to reach 0.67 maximum wetting force. Steam aging increases this wetting time further for most coarse-grained solder-coated wires. Examples of wetting curves for a coarse-grained, solder-coated wire before and after steam aging are shown in Figure 5. The dependence of wetting time before and after steam aging on the coarseness of the solder coating is shown in Figure 6. The variability in wetting times seen for as-received, coarse-grained solder-coated wires may be due in part to a variable storage time after plating before the wire was tested. After 24 hours of steam aging, nearly all of the wire coated with coarse-grained solders require more than 2 seconds to reach 0.67 maximum wetting force. The change in wetting time with steam aging duration is shown in more detail in Figures 7 and 8. Most of the increase in wetting times for wires with coarse-structured coatings is seen to occur in the first 8 hours of steam aging.

Reflowed solder coatings have been produced on nickel wire by GTE Products Corporation. For wire originally coated with fine-grained solder, a coarsening of the solder microstructure occurs during reflow (mean intercept distance 2 to 3 μm after reflow). The thickness of the solder coating after reflow is specified by GTE to be 1.5 to 12.7 μm (60 to 500 μ in.); samples tested in this study generally had coating thicknesses from 5 to 10 μm (200 to 400 μ in.). The time to reach 0.67 maximum wetting force is slightly greater than the original plated wire. As is the case for the original fine-grained, electroplated wire, no increase in wetting time is seen with steam aging for these wires (Figure 8).

Wire dipped in molten 60 tin - 40 lead solder after burn-in was of intermediate grain size (Figure 9) and had a coating thickness ranging from 1.5 to 6.3 μm (60 to 250 μ in.). Significant thickness variation was seen at different regions of a given sample. The time to reach 0.67 maximum wetting force varied from 0.5 to 1.9 seconds shortly after dipping and increased to 2 to 2.5 seconds after 24

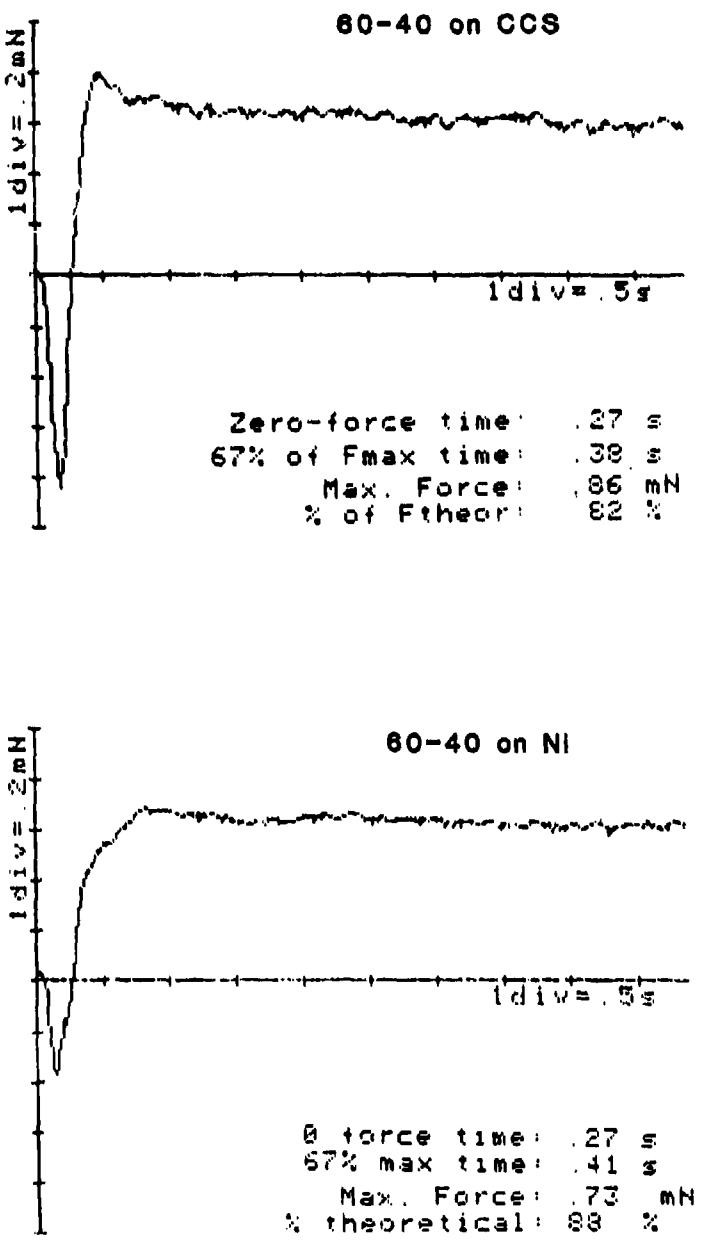


FIGURE 4. Typical Wetting Curves of GTE Products Corporation Wires Coated with Fine-Structured Solder

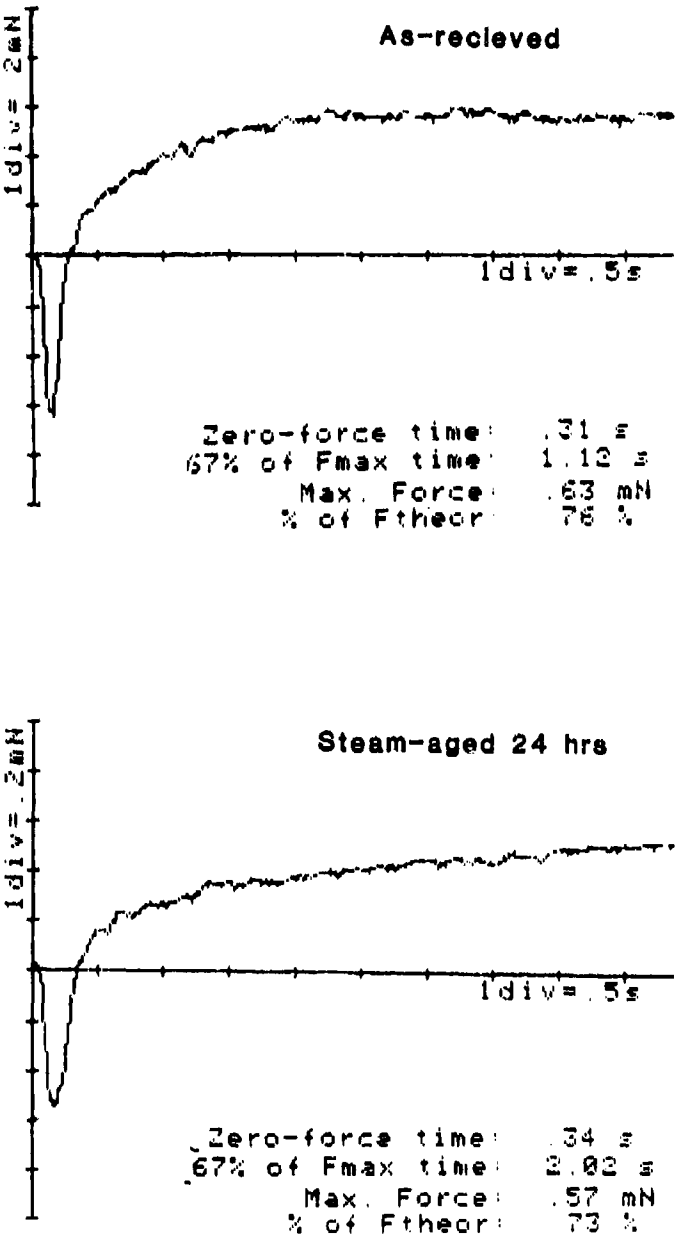


FIGURE 5. Typical Wetting Curves for Wires Coated With Coarse-Structured Solder (60 Sn-40 Pb on CCS)

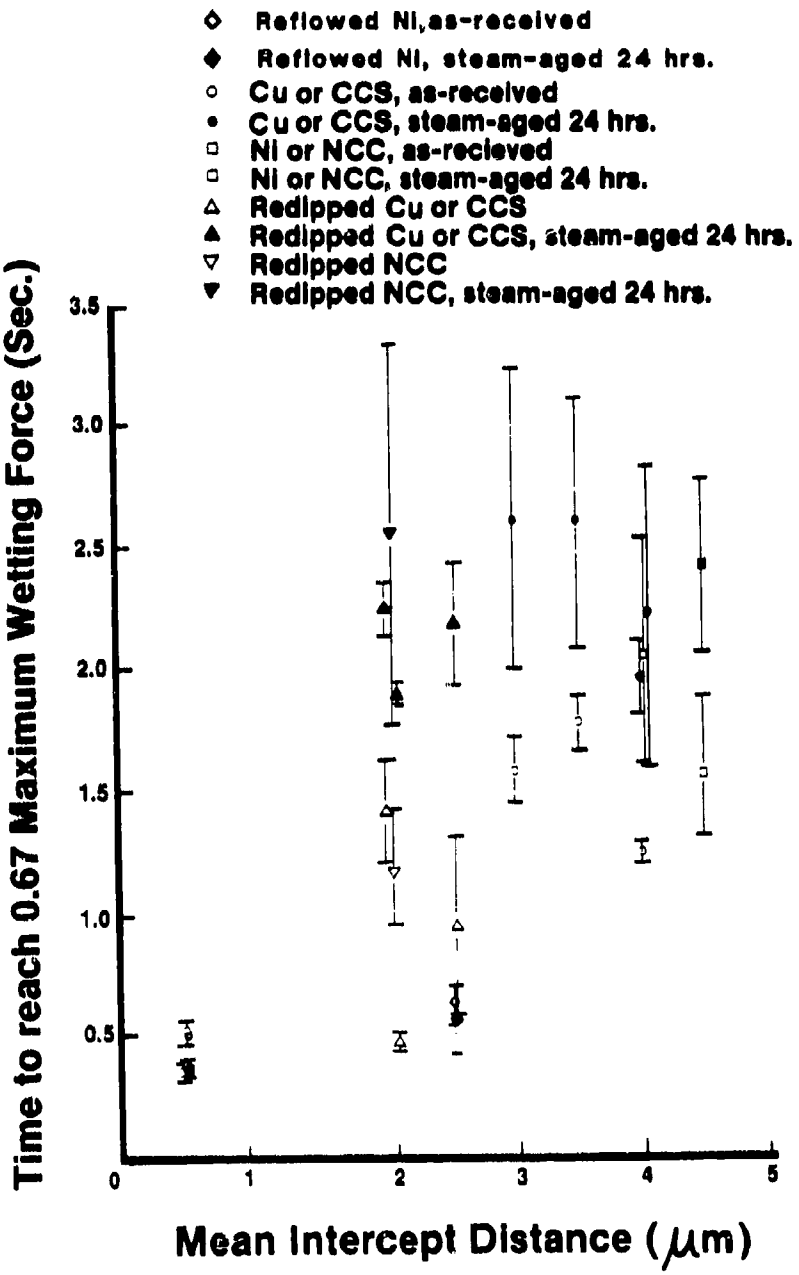


FIGURE 6. Wetting of 60 Sn - 40 Pb Solder-Coated Wires Before and After Steam Aging vs. Coarseness of Solder Coatings.

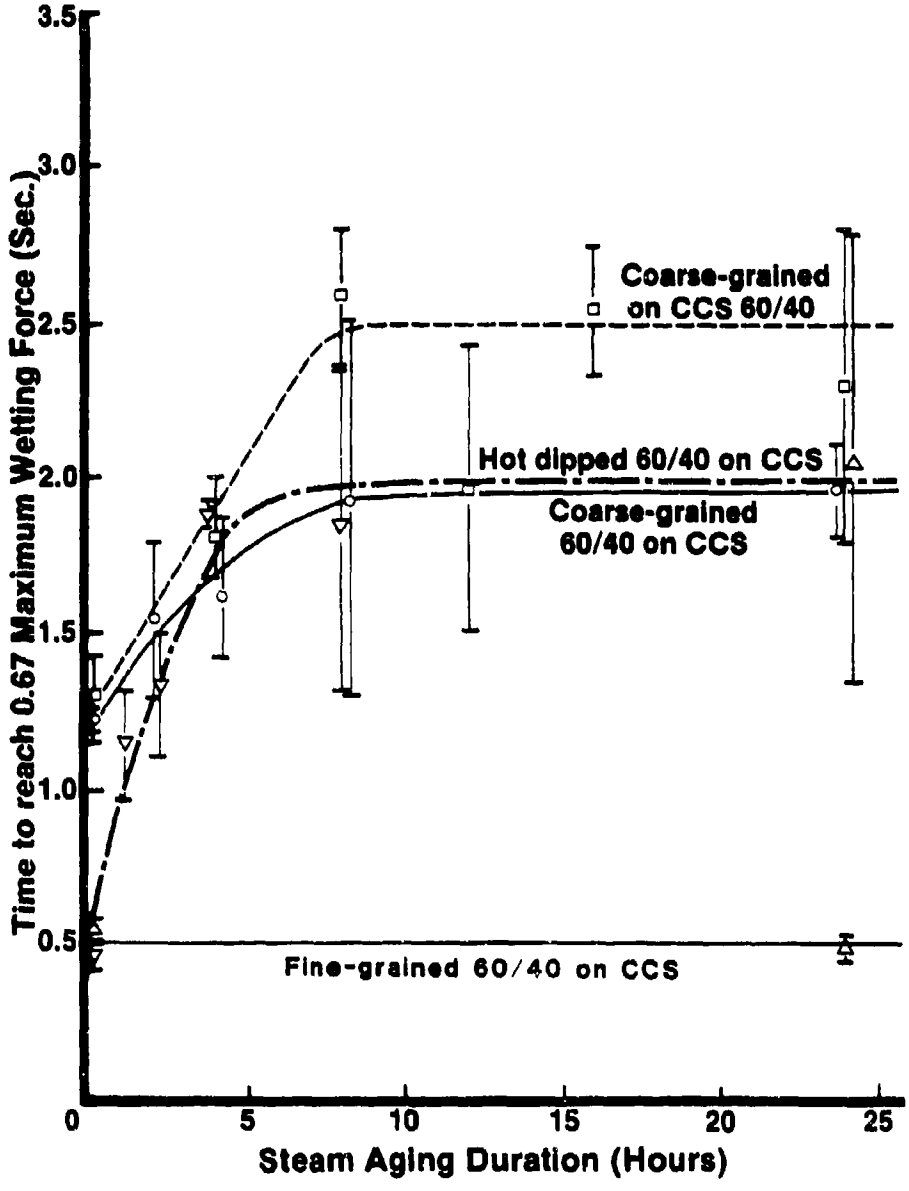


FIGURE 7. Effect of Steam Aging Duration on Wetting Time of Solder Coated Copper-Clad Steel Wires.

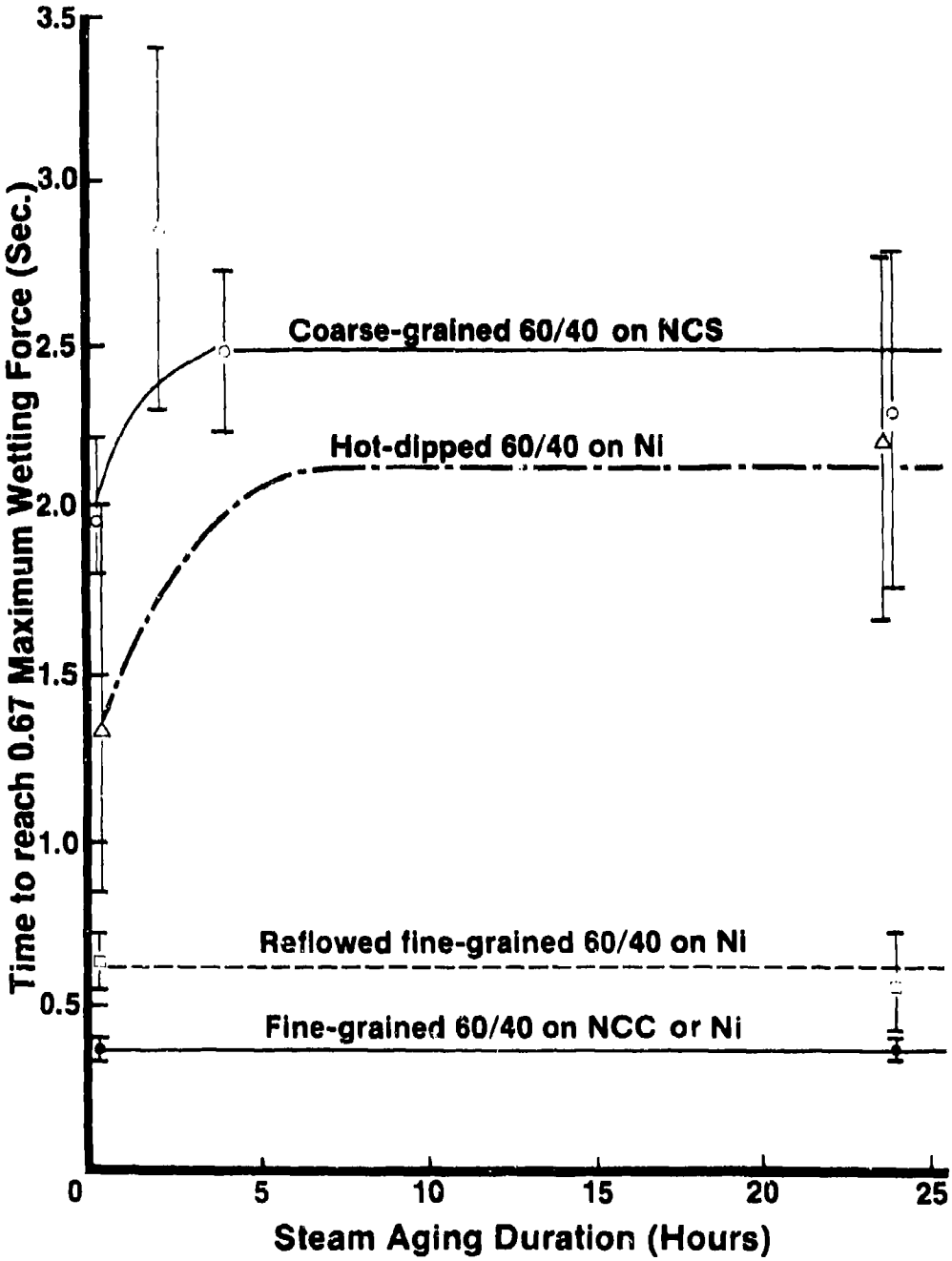
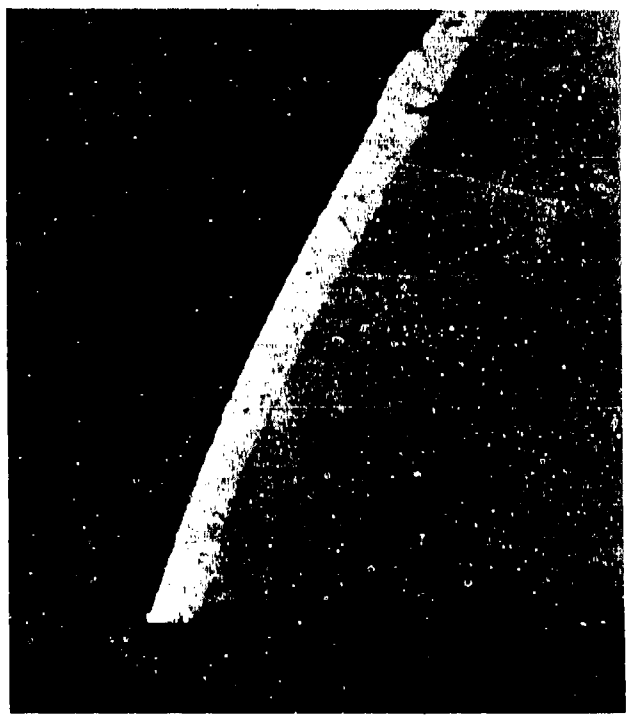


FIGURE 8. Effect of Steam Aging Duration on Wetting Time of Solder Coated Nickel and Nickel-Clad Wires.

hours steam aging (Figures 7 and 8). Examples of wetting curves on hot-dipped wire samples before and after steam aging are shown in Figure 10. The superior performance claimed for hot dipped coatings (References 4 and 5) were, thus, not found in this study. The thinner coatings produced by hot-dipping may be responsible for their relatively slow wetting after steam aging.



60-40 on NI

FIGURE 9. Backscattered Electron Image of Polished Cross-Section of Wire Dipped in Molten 60 Sn-40 Pb Solder

All wire samples examined had at least 95% coverage after immersion in 60 tin-40 lead solder at 245 deg.C for 5 seconds, even after 24 hours steam aging.

CORE COMPOSITION AND INTERMETALLIC COMPOUND GROWTH

No differences in solderability of copper and nickel wire coated with equivalent solder coatings was detectable. Burn-in testing at 85 deg.C for 40 hours does not

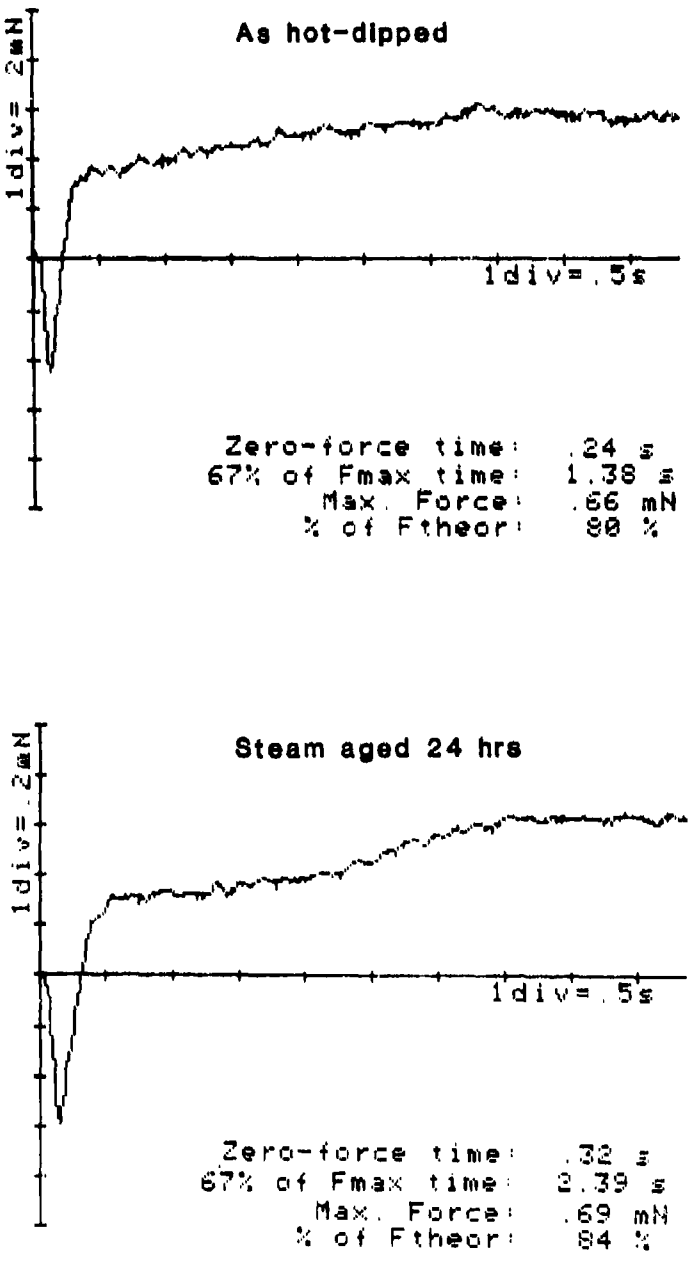


FIGURE 10. Typical Wetting Curves for Lead Wire Hot Dipped in Molten 60 Sn-40 Pb Solder (CCS)

significantly change the wetting characteristics of any of the wires. Burn-in testing at 125 deg.C for 100 hours, which produces a 1 μm (40 μ in.) thick intermetallic compound layer in nickel wire and a 2 μm (80 μ in.) intermetallic layer in copper wire, results in a moderate decrease in wetting speed for some wires and has no effect on others. Effects of burn-in appear to be similar for copper and nickel core wires and are generally less severe than the effects of steam aging. This implies that the increase in wetting times seen with elevated temperature exposure is due primarily to oxidation rather than growth of intermetallic compounds. The plating method used by GTE to manufacture fine-structured solders apparently produces a coating less permeable to oxygen than plating methods used in the manufacture of coarse-structured coatings.

CAPACITOR FABRICATION

Lead wires on Kemet tantalum and film capacitors are attached using near-eutectic solders at about 200 deg.C. These processes do not have any detectable effects on the solder coatings of the lead wires in regions where they are soldered to circuit boards (≥5mm (0.2 in) from the capacitor case). Lead wires on hermetically sealed (canned) tantalum and film capacitors have wetting characteristics identical to the original wire materials. Molded parts are "deflashed" by an abrasive process after molding, which removes some of the solder coating near the case. This causes some decrease in wetting speed of the leads. Wires with fine-grained solder coatings retain a significant advantage in wetting speed over wires with coarse-grained coatings on molded parts, however, and still generally reach 0.67 maximum wetting force in less than 1 second.

Ceramic capacitors are required to survive soldering at temperatures up to 250 deg.C, so high melting point solders are used for lead attachment. These lead-attach processes cause some melting of the solder coatings on the lead wires, modifying their thickness and microstructure. The effect of this on lead-wire solderability is under investigation.

CONCLUSIONS

1. The wetting speed of solder-coated wire is correlated with the microstructure of the solder coating. Wires coated with coarse-grained solders wet relatively slowly and are degraded by steam aging. Wires coated with fine-grained solders wet very rapidly and are unaffected by steam aging.

2. For wires with coarse-grained and hot dipped solder coatings, time to reach 0.67 maximum wetting force increases with steam aging duration up to about 8 hours; after 8 hours, little change is seen with additional steam aging.

3. Hermetically-sealed tantalum capacitors made using wire coated with fine-grained, electroplated solder, or reflowed, fine-grained solder have lead wires which exhibit wetting characteristics superior to those of leads hot-dipped after fabrication, particularly after steam aging.

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SOLDERABILITY DEFECT ANALYSIS

- SIMPLIFIED

by

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Syracuse, New York

November 1985

ABSTRACT

In 1982, a failure analysis technique known as solderability defect analysis was formalized and published. The technique was fairly complex and required a number of analytical steps to complete. The purpose was to define exactly the cause of poor solderability on a component part or printed wiring board. This information could then be used to correct the problem through rework or to provide information to vendors to help them correct their processes.

In the past three years an effort has been made to simplify the technique in order to promote a more widespread use. We are now able to provide an adequate answer within one-half hour of receipt of the samples.

The simplification process has been achieved through the use of the wetting balance solderability test. It has been found that test curve fine structure will provide a generic answer to the cause of poor solderability. When this is coupled with the information from the scanning electron microscope/electron microprobe analysis, an exact cause can be determined.

This paper describes the details of the technique, the samples required and the basic important details of the wetting balance curves needed to make determinations. Also included will be a number of case histories which show practical use of the technique.

Introduction

Approximately two years ago, a method was developed[1] which we called "Solderability Defect Analysis." The purpose was to provide accurate information on the cause of poor solderability of a particular component lead. This information could then be used to inform the component vendor where the problem had occurred in his process. The success of the method was dependent upon good SEM and chemical analysis information. This did not detract from the usefulness of the method but did limit the ability to use it frequently. This was due to the limited availability of equipment and the cost associated with it.

Since 1982, we have continually worked to upgrade solderability defect analysis techniques. These efforts were mainly directed at reducing the time and cost of analysis, as well as improving its accuracy. The remainder of this paper describes our latest techniques. Case histories are shown to illustrate technique application.

Basic Technique

The technique of solderability defect analysis is now based on the use of the wetting balance. In our work to fully identify the mechanisms of solderability[2], it was found tht the fine structure in the resultant wetting balance curve gave extremely useful information as to the nature of a solderability problem. Correlating what we saw in the wetting balance with the physical evidence obtained using scanning electron microscope/electron microprobe techniques, it was found possible to fairly accurately define the cause of poor solderbility.

Interpretation of wetting balance curves can give the following information.

1) The mechanism of solderability operating.

2) The depth at which a defect resides.

3) The general nature of the defect.

In many cases, this is sufficient information to get a vendor back on track to providing parts with good solderability. The technique has been applied to both component leads and larger but fully wettable terminations.

The data from the wetting balance can then be supplemented with both optical inspection and SEM/EMA analysis if the equipment is available.

Interpretation of Wetting Balance Curves

Since the technique of solderability defect analysis is reliant on wetting balance curves, the generation and interpretation of them is all important.

The basic factor in the generation of the curve is the ability to detect fine structure. Therefore, the physical size of the curve generated must be large enough to read. The vertical sensitivity must be high enough to detect differences of 2-3 dynes (Nm). The horizontal scale must be such that a 10 sec test time is stretched to 4-5 inches. If a chart recorder is used, then the sensitivity should be 50 mv/sec or better and the chart drive (or pen drive) should be 15-20 inches/min or faster. If a computer is used, the important factor is sampling rate. The sample rate should be at least 30 times/sec.

Once the curve is generated, the next step is interpretation. The following is a list of important indications to look for in a curve.

1) Wetting time (time for the curve to cross the zero axis).

2) Wetting rate.

3) Changes in wetting rate and where they occur.

4) Wetting force at 1 and 2 seconds, at equilibrium, and at test completion.

5) Lack of smoothness in the curve and where it occurs.

6) Withdrawal force.

7) Solderability number[3].

8) Identification of artifacts in the curve.

For good solderability, wetting times should be short; characteristically, well under 1 second. Longer wetting times indicate a non-reducible film has been encountered. Typically, this is usually an oxide or a stable organic film.

The wetting rate is the indicator of how rapidly the metallurgical reaction at the surface is taking place. This should be very rapid for good solderability; characteristically, it should be 300 dynes/sec or faster. Slow wetting rates indicate a fairly stable oxide is being reduced or removed slowly.

Changes in wetting rate are a very important indicator. By use of this information, a defects location may be determined. Typically, one

notices this effect on plated parts. The most common effect is to see a very fast initial wetting rate which suddenly changes to a slower wetting rate. This shows that the surface plating is very wettable or alloyable. Once the solder reaches the interface between the surface plate and the metal underneath, the wetting rate of that surface will be seen. If it is "clean", no change in rate will be noted. However, if it is "dirty", the wetting rate will slow down. This usually indicates poor cleaning prior to final plating. By noting the time between initial wetting and the change in rate, the location of the defect can be estimated.

Wetting force evaluation is the next important indicator. The wetting force is an indicator of the quality of metallurgical wetting. Complete and uniform wetting will give high wetting forces; usually over 275 dynes/cm. Less then this will indicate incomplete or non-uniform wetting. Since most of our production soldering processes are operated on the basis of 1-5 seconds contact time with the molten solder, it is important that maximum wetting takes place in this time. Based on this, we prefer to see nearly maximum wetting in 2 seconds or less. Therefore, we like to see the wetting force above 250 dynes/cm at 2 seconds. Less than this indicates non-reducible materials at the solder bond which could affect joint strength or life (i.e., fatigue).

Lack of smoothness in the curve most often indicates gas evolution. As the bubbles of gas are released and interface with the meniscus, the wetting force goes up and down. Since the evolution of gas is part of the dewetting mechanism, this is an important factor to note. It should be said that not all gases cause dewetting but they can introduce voids into a solder joint. The lack of smoothness in the curve is most often noted at the knee.

The most reliable indicator of dewetting we have found to date is the withdrawal force. This force is measured from the maximum wetting force. Typically, we like to see this force less than 100 dynes/cm. Greater than this indicates significant dewetting has occurred. Typical defects causing dewetting are organics in plated coatings[4] and water of hydration in inorganics (i.e., hydrated oxide). Many times the gas evolution indicators and the dewetting indicator can be correlated to estimate defect location. This is not quantitative and takes some experience.

Effects of artifacts on the curve must be subtracted during the curve evaluation. Artifacts can come from obvious sources such as impacts or excessive vibration during test, poor recording equipment or tester malfunction. One artifact often not recognized as such is a drop in the curve after the knee. This, in reality, is most often a flux function not related to the sample under test. Since all testing for solderability defect analysis should be done with type "R" flux, the drop most often occurs when too much flux is used. Physically, what

happens is that the excess flux runs away from the area of the sample. This draws much of the flux away from the area of the meniscus allowing surface tension to rise and wetting force to drop. When such a drop is noted, always look at the surface of the solder pot near the sample. To prevent this problem from occurring, always use a thin film of flux and make sure that there is not a droplet of flux on the end of the lead.

Supplementary Techniques

The major supplementary technique is solderability defect analysis is scanning electron microscopy and electron microprobe analyses (SEM/EMA). The details of this technique may be found in my previous paper[1]. The major advantge of using SEM/EMA is to more accurately define the cause of the defect.

Optical microscopy is also useful and generally available to everyone. Both the low power stereo microscopes and the higher power metallurgical microscopes fall into this category. As a minimum, the sample which had been wetting balance tested should always be examined with a stereo microscope. Much useful information can be collected this way. An excellent example is shown in the case histories.

Relations with Vendors

The rules in dealing with vendors are fairly simple but quite rigid. The first rule is to deal on the technical level only. This requires getting past the purchasing/marketing organizations. The second rule is having hard technical data in your hand. This what "Solderbility Defect Analysis" is all about. The third rule is to inspire cooperation rather than conflict. Obeying rule two goes a long way toward this objective. As a corollary, it should be instilled that it is to both parties benefit to solve the problem.

Case Histories

1. Transistor Leads

The leads on transistors from this vendor had a history of poor solderability as evidenced by a high solder joint touchup rate. The leads are tin plate over alloy 42. Figure 1 shows the wetting balance trace. The major features seen in the curve are a change of wetting rate and a high withdrawal force. The analysis of wetting rate shows that the tin plate wet very fast. As soon as it was alloyed off, wetting rate slowed down dramatically indicating the problem was at the tin plate/base metal interface. The high

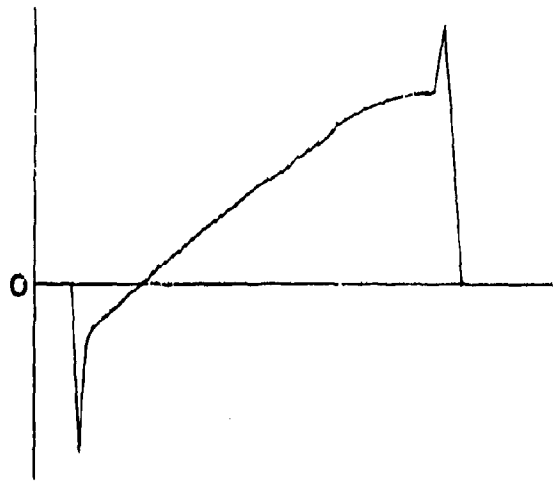

Figure 1

withdrawal force showed dewetting to be the problem. In other words, dirty base metal prior to plating. Discussions with the vendor located the exact problem. The lead frame is processed in machinery using a die lubricant of silicones.

2. Copper Lugs

Tin plated copper lugs from one vendor were found to be hard to solder. When soldered, the joints had very low strength. Figure 2 shows the wetting balance trace.

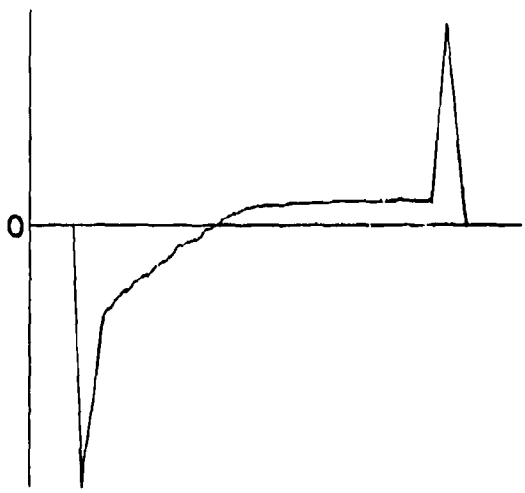

Figure 2

The curve shows slow wetting (5.2 seconds), wetting rate change, low wetting force and high withdrawal force. The analysis of the curve indicated a non-wetable material at the tin plate/base metal interface. This same material caused significant dewetting. SEM/EMA analysis located the exact problem. Figure 3 shows the solderability tested surface. Microprobe analysis showed the "rocks" were aluminum oxide and were embedded in the copper. The conclusion was that tumbling media used for deburring of the stamped tabs was being embedded and not removed prior to plating.

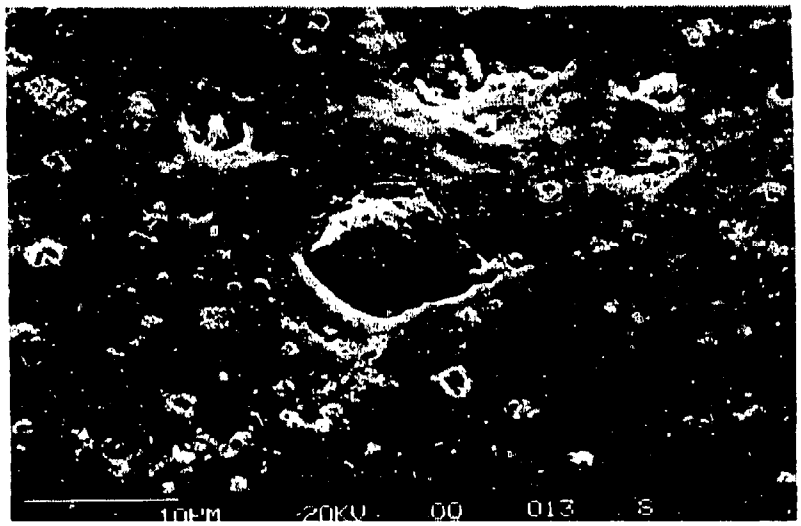

Figure 3

3. IC Flatpack

The leads of a flatpack package were to be evaluated for solderability. These were gold plated over 42 alloy base metal. Figure 4 shows the wetting balance trace taken. The main feature is that the trace never rose above the zero axis when tested for 5 seconds-

This indicated something on the surface of the gold plate was non-wettable. SEM examination showed a very stable organic on the surface. This was in two forms as shown in Figure 5. The worst was the heavy deposit which caused non-wetting. The second was more stain-like which caused dewetting. Optical examination of the solderability tested samples showed the spots were in distinct lines across the leads. This can be seen in Figure 6. The conclusion was contaminated test fixtures used by the package manufacturer.

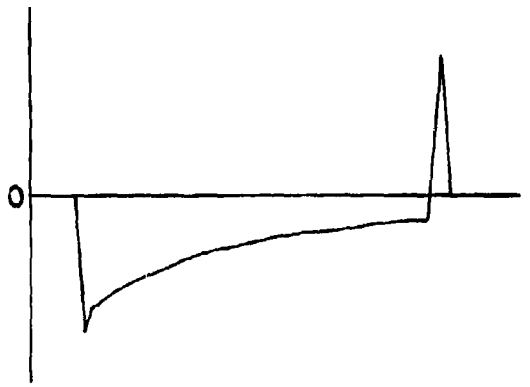

Figure 4

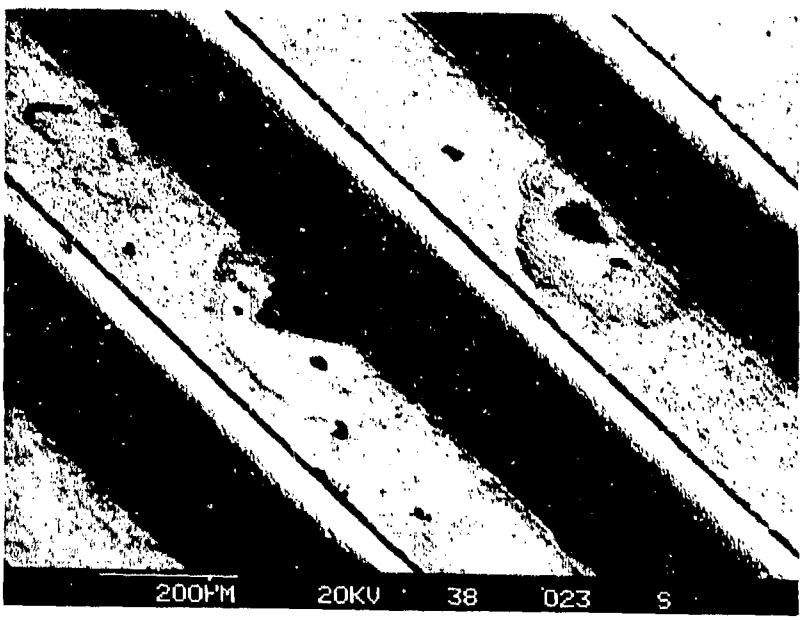

Figure 5

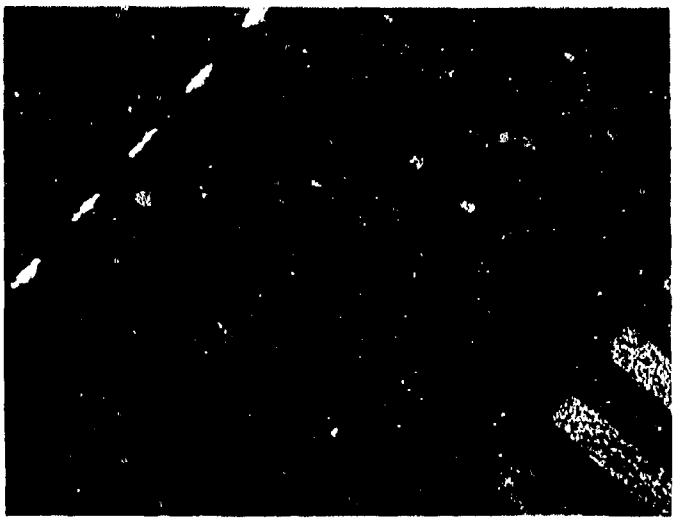

Figure 6

Summary

1. "Solderability Defect Analysis" is a very useful technique in solving problems of solderability "up front."

2. Through the use of the wetting balance, the technique is available to both users and vendors. It can be performed on a routine basis at low cost.

3. The technique can now be used to identify the generic nature of a defect causing bad solderability very rapidly (often in less than one-half hour).

4. For complete identification of a defect, it is necessary to use the supplementary analysis techniques of SEM/EMA, cross-section and optical microscopy.

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SOLDER DEFECT MODE ANALYSIS UNDER THE "ZERO" DEFECT CONCEPT

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DYNAMIC MECHANICAL TESTING OF SOLDER AND SOLDER JOINTS

by

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ABSTRACT

Successful use of solder joints to attach surface mounted devices to printed wiring board substrates requires knowledge of the stress-strain properties of solder as functions of temperature, time, and loading conditions. In addition, the relatively high operating temperature of solder in comparison to its absolute melting temperature introduces a requirement for an understanding of the influence of creep effects on the mechanical properties of solder under cyclical loading conditions. In the past, studies of these solder properties have been limited by the need to use relatively large bulk solder samples that may or may not be representative of actual solder joints in a printed wiring board-chip carrier environment.

A previously unreported test method for the evaluation of the dynamic mechanical properties of solder and solder joints has been developed. The method is based upon the use of a Rheometrics Dynamic Spectrometer, which has been shown to be capable of determining both the elastic and plastic responses of solder joints during cyclical loading under a variety of imposed strains, strain rates, and temperatures that are within the range of anticipated service conditions. In addition, stress relaxation properties of solder joints may be studied.

INTRODUCTION

Solder joint reliability continues to be one of the most critical technical issues in surface mount technology development, since the solder joint serves as both the mechanical and the electrical link between the component and the printed wiring board. Although a variety of factors may cause solder joint failures, it is generally recognized that the primary source of failure is low cycle-strain-controlled fatigue that arises when the assembly is subjected to temperature variations (References 1-6). Such conditions as ambient temperature changes, power dissipation in chip carriers, and power on/off will, when combined with the unequal thermal properties of the component and the printed wiring board materials, result in stresses and strains that can ultimately result in solder joint failure.

Cyclic fatigue damage in solder joints has been related to creep or stress relaxation effects that occur when solder is subjected to a strain at normal service conditions (Reference 7). The presence of significant creep effects is, in turn, due to the relatively high service temperature of solder in comparison to its reflow temperature. The amount of damage that occurs in a given cycle is both time- and temperature-dependent. These characteristics can have significant consequences for any attempt to design either an analytical or an experimental program to investigate solder joint reliability. It is therefore necessary to address both the elastic and the inelastic (creep or stress relaxation) responses of solder in order to fully understand the mechanical behavior of solder joints under cyclical loading conditions.

EXPERIMENTAL

DYNAMIC MECHANICAL ANALYSIS OVERVIEW

Dynamic mechanical analysis is a technique that may be used to measure the ability of a material to store and dissipate (through relaxation processes) mechanical energy. When a material such as solder is subjected to a sinusoidally varying strain, the resultant stress will also change in a sinusoidal manner. However, the stress will not be in phase with the strain due to the presence of stress relaxation processes in the solder, but instead is shifted in phase by an angle δ. This is illustrated in Figure 1A. The stress response can be mathematically described as the combination of two separate sinusoidal waves, one of which is in phase with the strain, and the other of which is exactly ninety degrees out of phase with the strain. The relative amplitudes of these two waves are dependent upon the value of δ. This is illustrated in Figure 1B. It can be shown, through arguments too complex to discuss in this brief overview, that the amplitude of the in-phase component of the stress response is related to the amount of energy that is stored elastically in the sample, and that the amplitude of the 90 degree out-of-phase component of the stress response is related to the amount of energy that is lost through an inelastic or plastic response, such as creep or stress relaxation (Reference 8).

Figure 2 shows a block diagram of a Rheometrics Dynamic Spectrometer (RDS-7700, manufactured by Rheometrics, Inc., Piscataway, N.J.), which is designed for dynamic mechanical testing of a wide range of materials. This diagram shows the signal flow and interconnection of major components. In operating the system, the user first clamps the sample between two fixtures, one of which is driven by a motor, and the other of which is rigidly mounted to a transducer. The user then selects the deformation that is to be applied to the sample by specifying both the strain and the strain rate (or sinusoidal test frequency) that is to be used. Samples may

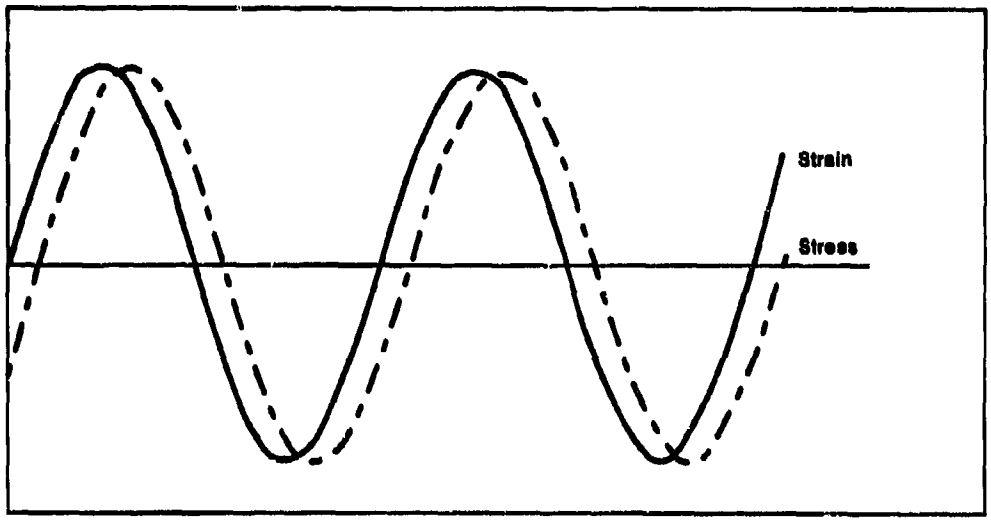

Figure 1A. The strain and resultant stress for a viscoelastic material are offset during dynamic mechanical testing.

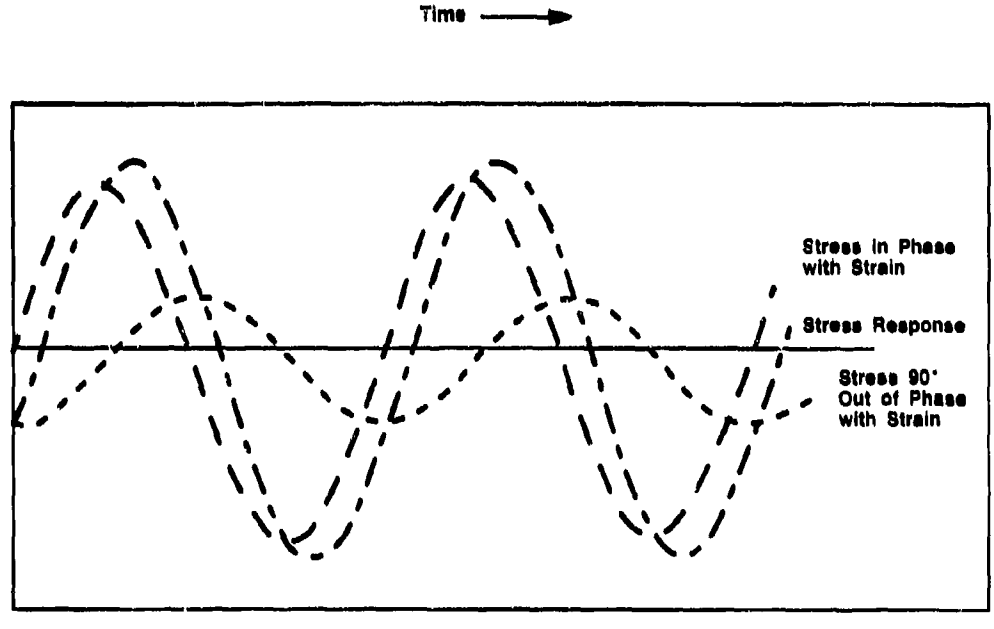

Figure 1B. The stress response in Figure 1A can be mathematically described as the sum of two stress components: one in phase with the strain, and the other 90° out of phase with the strain.

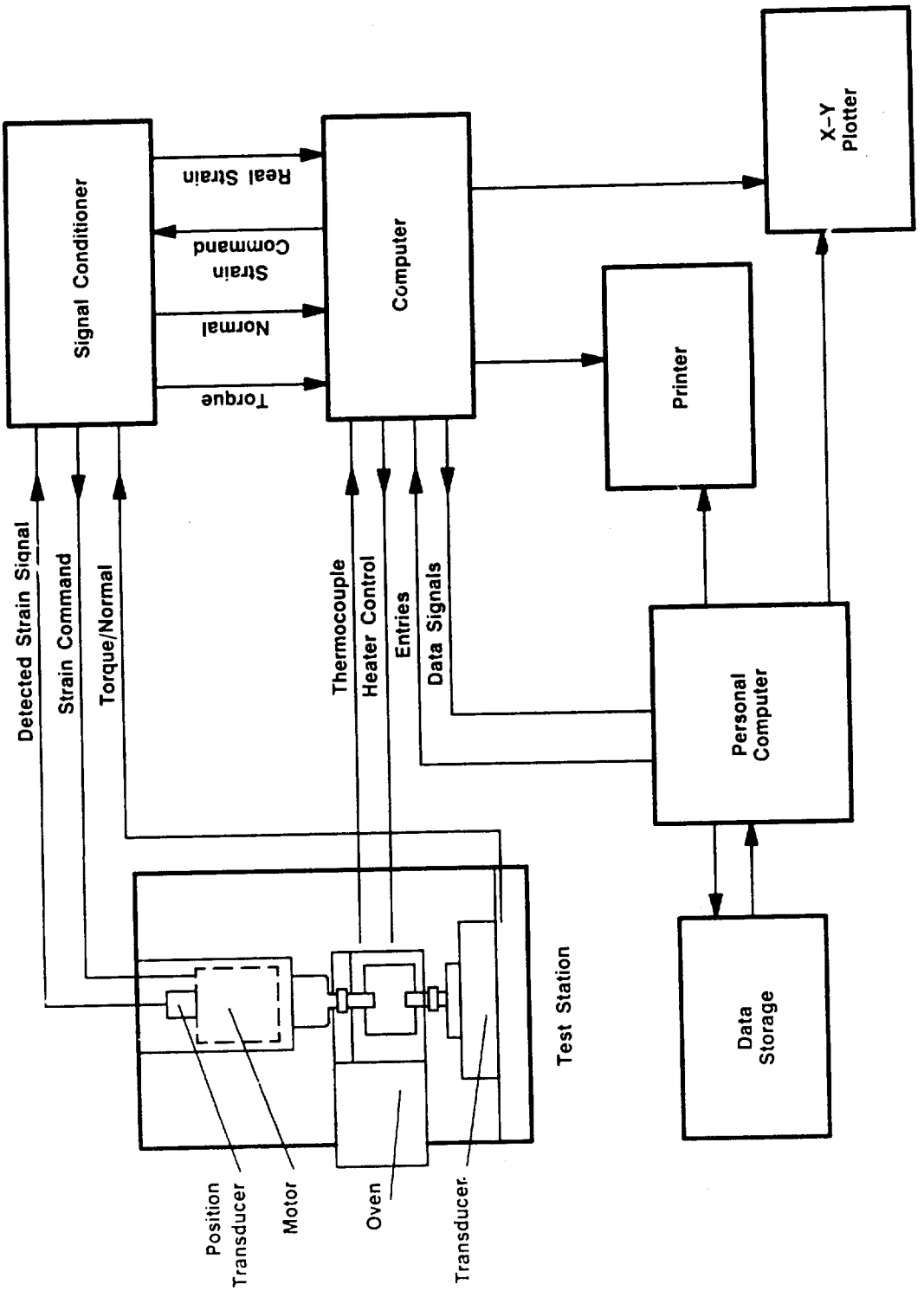

Figure 2. Block diagram of the rheometrics dynamic spectrometer (RDS-7700).

be tested in shear or tension-compression. Alternatively, step strains may be applied for direct stress relaxation studies. A precision motor controlled by a position servomechanism applies a deformation to the material, with the frequency and amplitude of the deformation controlled by the central processor. The actual strain is measured using a position transducer that is coupled directly to the motor shaft. This eliminates possible errors due to servo dynamics.

The torque and the normal force that are generated in response to this imposed motion are measured by the transducer. For the work reported in this paper, a temperature-controlled transducer with a maximum normal force load of 2000 grams was used. The deformation force signals, plus the strain signal, are amplified and input to the central processor. The central processor contains a sampling sine wave correlator which rejects both harmonics and noise, and calculates the values of the elastic and inelastic components of the deformation process based upon the peak magnitude of the force and the phase angle shift between the stress and the strain. The temperature is controlled throughout the test using convected gas in an environmental chamber that surrounds the sample.

BULK SOLDER TESTS

Tests on bulk solder were conducted with 1.1" x 0.2" x 0.065" cast solder bars. Each solder bar was polished to a 600 grit finish, with polishing performed in the longitudinal direction to avoid premature crack nucleation during testing. The solder bars were directly loaded into the RDS-7700 and were tested in a tension-compression mode.

SOLDER JOINT TESTS

Several types of fixtures were designed, fabricated, and evaluated for solder joint testing. The final test fixture design is shown in Figure 3. The test fixture, which was fabricated from stainless steel, is composed fo two identical halves. In use, a single chip carrier-solder joint-substrate assembly is attached between the two fixture halves by using a rigid epoxy adhesive on the back of the substrate and on top of the chip carrier. The two fixture halves, with the solder joint assembly between them, are then mounted in the tension-compression fixture of the RDS.

The chip carrier-solder joint-substrate sample that is used in the test procedure is shown in Figure 4. Note than the chip carrier and the substrate are attached by only two solder joints that are directly opposite one another. These solder joints carry the entire applied load during the test. The imaginary line between the two

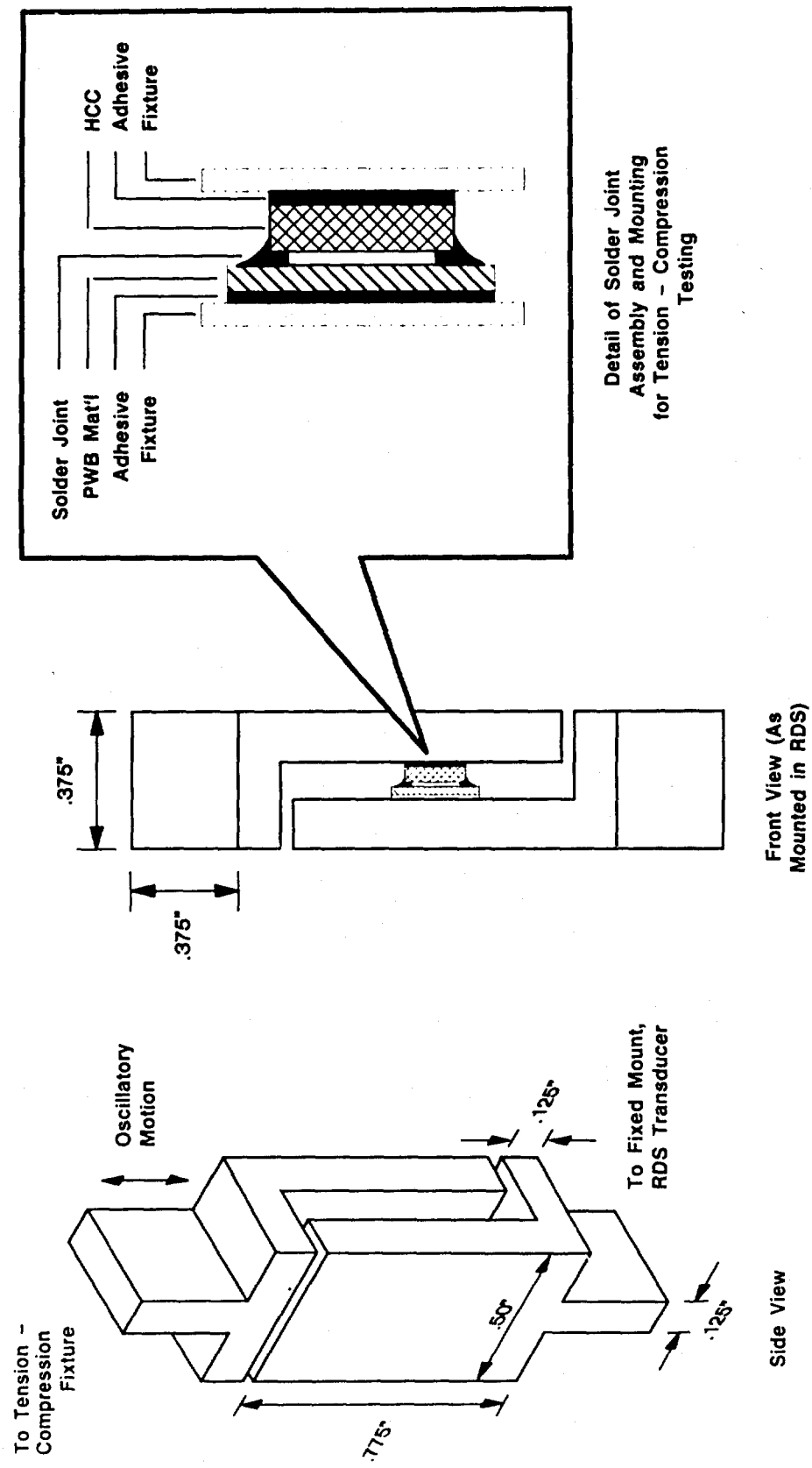

Figure 3. Solder joint test fixture - final design.

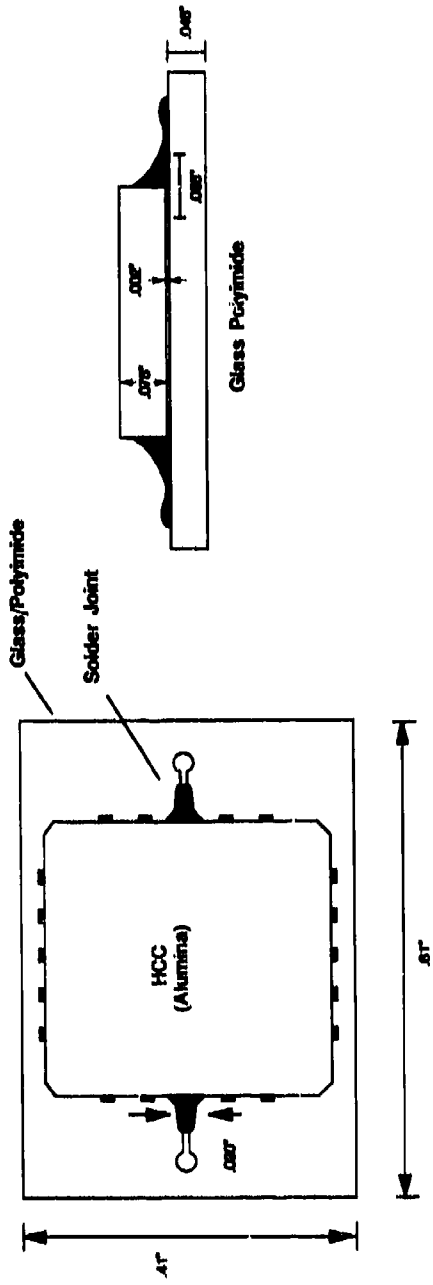

Figure 4. Solder joint test assembly.

solder joints is placed parallel to the direction of movement of the tension-compression fixture during testing. When loading the test fixture, the torque and normal loads on the transducer are carefully monitored to ensure that the solder joints are not subjected to stresses prior to test initiation.

RESULTS AND DISCUSSION

DYNAMIC MECHANICAL TESTING OF SOLDER BARS

Figures 5 and 6 show the results of frequency sweeps on Sn63-Pb37 and Sn62-Pb36-Ag2 solder bars, respectively. In this mode of testing, the frequency of the sinusoidal deformation that is applied to the solder is varied, while the strain remains constant. Note that this is equivalent to studying the response of solder to varying strain rates. The tests results that are shown in Figures 5 and 6 were obtained at 30 degrees C with a strain of 0.25%.

Examination of the test data shows that the elastic modulus of solder, while dependent upon solder composition, is fairly independent of strain rate at room temperature. The loss modulus, which is a measure of the extent of inelastic or plastic response of the material, is, however, dependent upon strain rate. Two distinct maxima are present in the loss modulus curves. The first of these occurs at or below a frequency of 0.01 radians per second (the minimum attainable frequency on the RDS), and the second occurs at a frequency between 1 and 10 radians per second. The higher values of the loss moduli in these two regions are indicative of the presence of two separate and strain-rate-dependent plastic response mechanisms in solder. This is consistent with slip (at high strain rates) and grain boundary sliding (at low strain rates) deformation modes.

In comparing the data in Figures 5 and 6, it can be seen that dynamic mechanical analysis is quite sensitive to changes in solder alloy composition. The presence fo 2% silver in a tin-lead alloy results in a large increase in the elastic modulus and a dramatic decrease in the loss modulus of the solder. The latter observation is particularly interesting, since a decrease in loss modulus is consistent with a decreased tendency toward inelastic deformation of solder in response to an imposed strain. Cyclic damage accumulation in solders has been related to the amount of grain boundary sliding that occurs in the alloy structure. The lower loss modulus of the Sn62-Pb36-Ag2 solder in comparison to the Sn63-Pb37 solder is consistent with less grain boundary sliding, and thus improved fatigue resistance, in the silver-containing alloy. This is consistent with results of actual thermal fatigue tests on surface-mounted components.

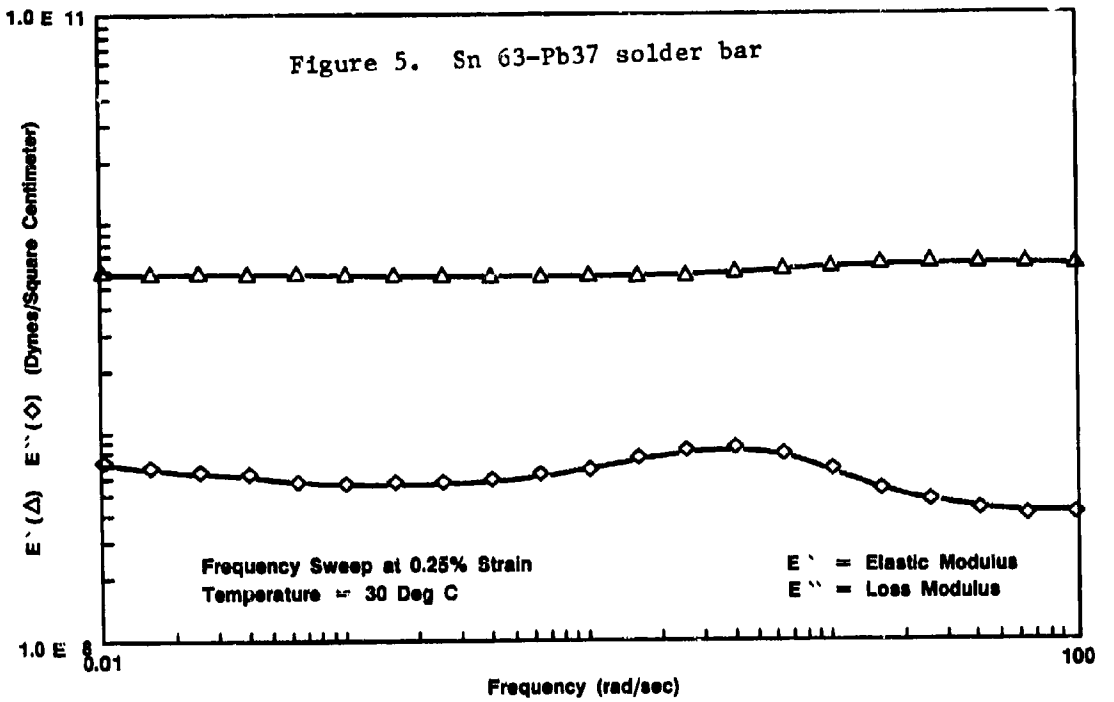

Figure 5. Sn 63-Pb37 solder bar

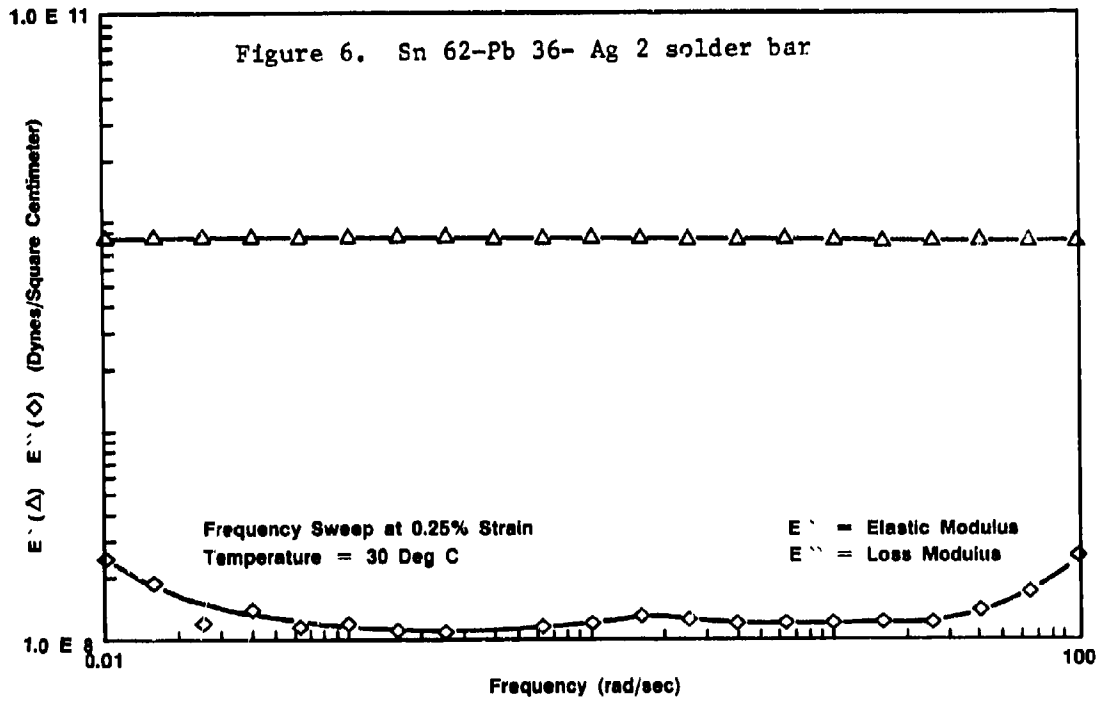

Figure 6. Sn 62-Pb 36- Ag 2 solder bar

The stress-strain response of solder bars as a function of applied strain at constant test frequency was also measured. Figure 7 shows the results of a strain sweep of Sn62-Pb36-Ag2 solder at 100 degrees C. The elastic modulus was found to be relatively independent of the strain. The loss modulus, however, was found to be strain-dependent under the same test conditions. In general, the value of the loss modulus was high at low strain levels, decreased as the strain was increased, and then began to increase as the strain was further increased. This behavior is once again consistent with the presence of two separate deformation mechanisms that are strain-rate dependent.

Stress relaxation tests wre also performed on solder bars. Figure 8 shows the results for stress relaxation tests for Sn63-Pb37 solder at -65 and 100 degrees C, respectively. Two interesting observations can be made from this data. First, stress relaxation in solder is a very lengthy process. Changes in the relaxation modulus (the ratio of stress to strain) were still occurring aftr 1000 seconds at both temperatures that were examined. This is consistent with the fact that the thermal cycling behavior of solder is dependent not only upon the rate and extent of temperature change, but also upon the hold time at the upper and lower temperature limits. In addition, it is interesting to note that, although stress relaxation is much more extensive at elevated temperatures, considerable stress relaxation can occur in solder even at -65 degrees C.

Figure 9 shows the effect of solder composition on the stress relaxation properties of Sn40-Pb60, Sn63-Pb37, and Sn62-Pb36-Ag2 solder alloys at 100 degrees C. Note that the two tin-lead solders are very similar in their stress relaxation behavior. The Sn62-Pb36-Ag2 solder, however, shows relatively little stress relaxation in comparison to the tin-lead solders. This is consistent with the superior fatigue resistance properties of the silver-containing alloy.

DYNAMIC MECHANICAL TESTING OF SOLDER JOINTS

During the initial evaluation of the dynamic mechanical properties of solder joints, two types of solder were tested. The first series of solder joints were prepared from a standard Sn62-Pb36-Ag2 solder paste. The other series of solder joints was also prepared from Sn62-Pb36-Ag2 solder. However, the alloy reportedly contained grain refiners for improved fatigue life.

Dynamic mechanical properties of the two types of solder joints were first examined by conducting frequency sweeps at 30 degrees C and strain of 0.5%. Test results for the two solders are compared in

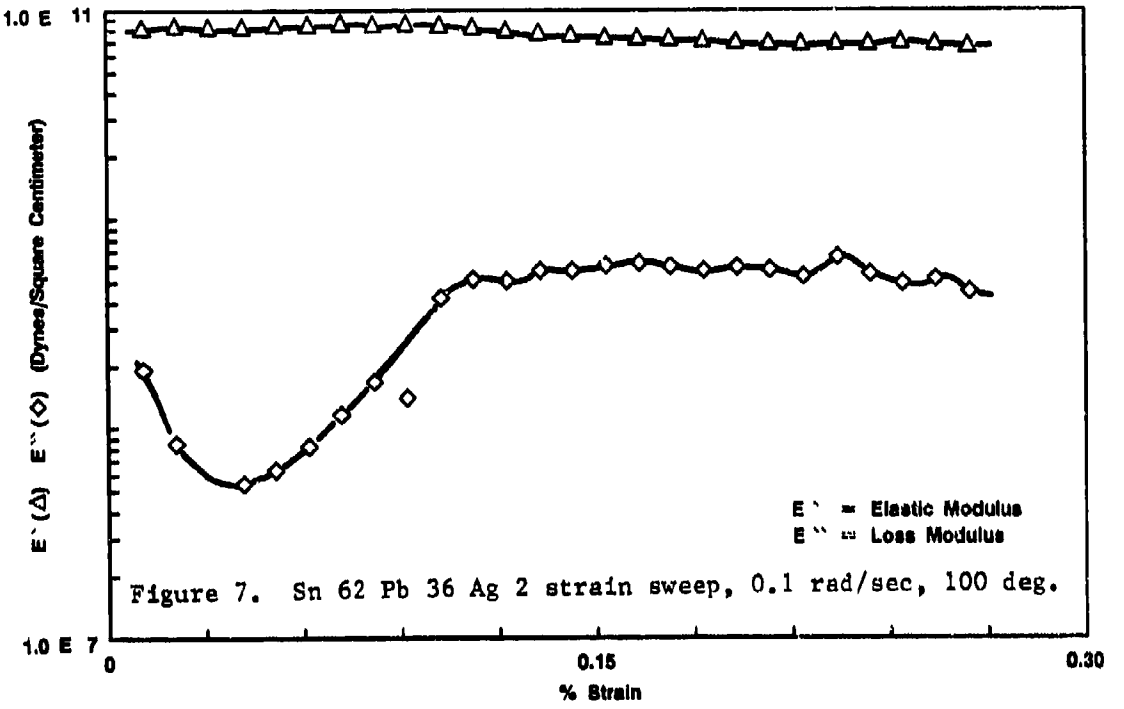

Figure 7. Sn 62 Pb 36 Ag 2 strain sweep, 0.1 rad/sec, 100 deg.

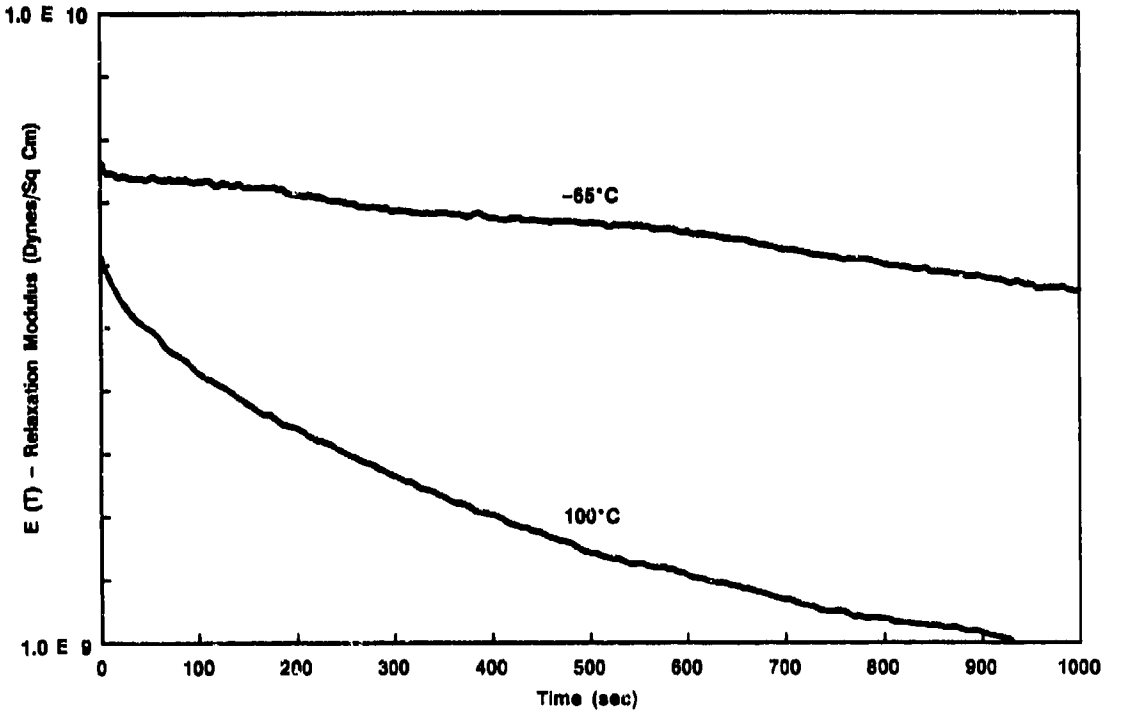

Figure 8. The effect of temperature on the stress relaxation of Sn63 - Pb 37 solder bars. Test mode: 0.1% step strain in tension.

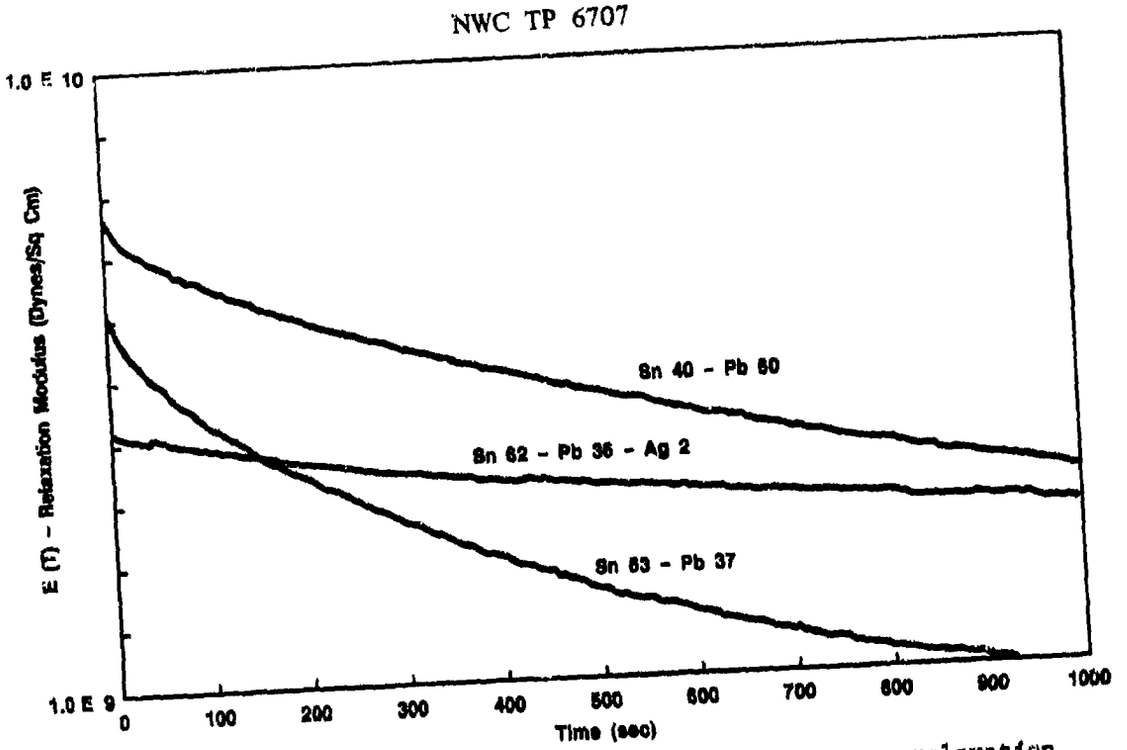

Figure 9. The effect of solder composition on the stress relaxation of solder bars-test mode: 0.1% step strain in tension at 100°C.

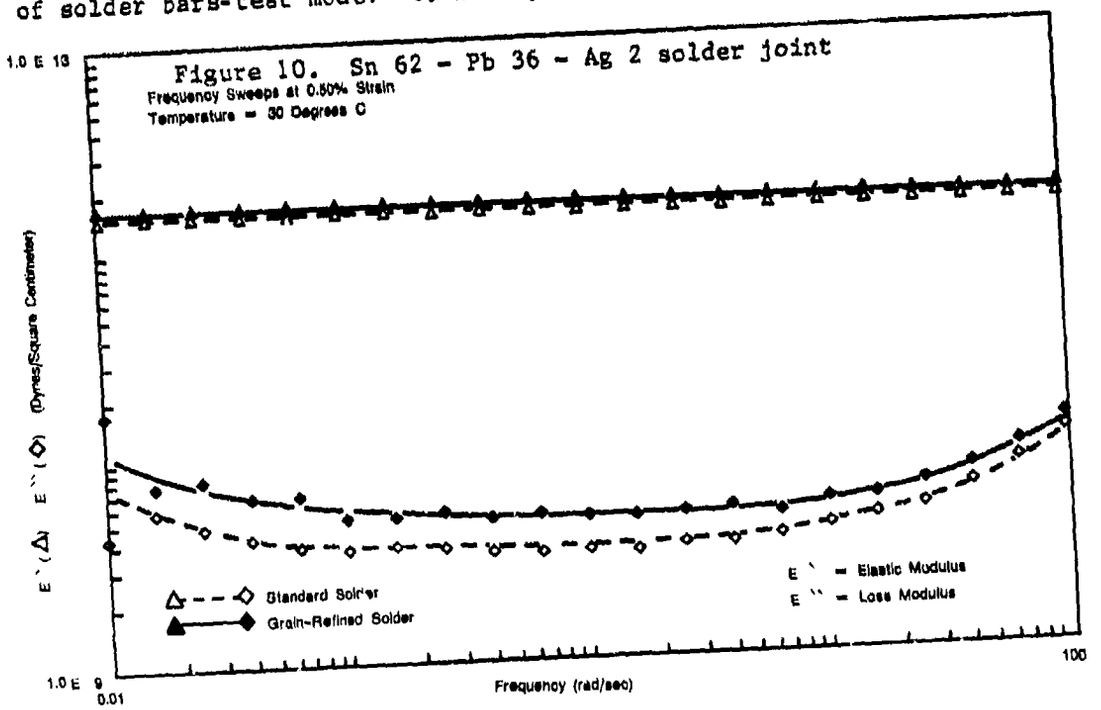

Figure 10. Note that in Figure 10, as in other data that was obtained on solder joints, only relative modulus values are reported. This is a result of the fact that, in order to calculate true modulus values, sample dimensions must be known. In the case of solder bars, the measurements of length, width, and thickness were straightforward. The complex shape of a solder joint, however, cannot be described by only three values. Therefore, a decision was made to input "ballpark" dimensional values into the RDS computer and to closely monitor solder joint geometries in order to ensure that valid comparisons could be made between different experiments. Particular attention was paid to ensuring that the stand-off height of the components was consistent from sample to sample by using small, removable shims under the component during the soldering process.

Examination of the data in Figure 10 shows that the dynamic mechanical properties of solder joints formed from the two different types of Sn62-Pb36-Ag2 solder are very similar at room temperature, with the elastic moduli being almost identical. The loss modulus of the standard solder is slightly lower that the loss modulus of the fatigue-resistant solder, particularly at low strain rates (low test frequencies).

The two solders were also compared at -65 and 100 degrees C. At -65 degrees C, the two solders have identical elastic moduli. The loss moduli for the two solders are below the detection limit of the RDS. At 100 degrees C, the elastic moduli of the two solders are again very similar. The loss modulus of the standard solder is somewhat lower than the loss modulus of the fatigue-resistant solder at low strain rates, with the differences between the two solders virtually disappearing as the strain rate is increased. This data is shown in Figure 11.

Based upon previous arguments, a relatively low loss modulus implies that only a small amount of grain boundary sliding occurs during deformation, and the solder would thus show less cyclical fatigue resistance than a solder with a higher loss modulus. The data in Figures 10 and 11 do not support the claim that the addition of grain refiners improves the fatigue life of Sn62-Pb36-Ag2 solder. Thermal cycling tests that were conducted on surface-mounted components subsequently confirmed that there was no significant difference in the fatigue behavior of the two solders.

Stress relaxation tests were performed on solder joints prepared from the standard Sn62-Pb36-Ag2 solder paste. Typical test results are shown in Figure 12. Note that the stress relaxation properties that were observed for solder joints varied from the results that were obtained for bulk solder bars (shown in Figure 9) in terms of

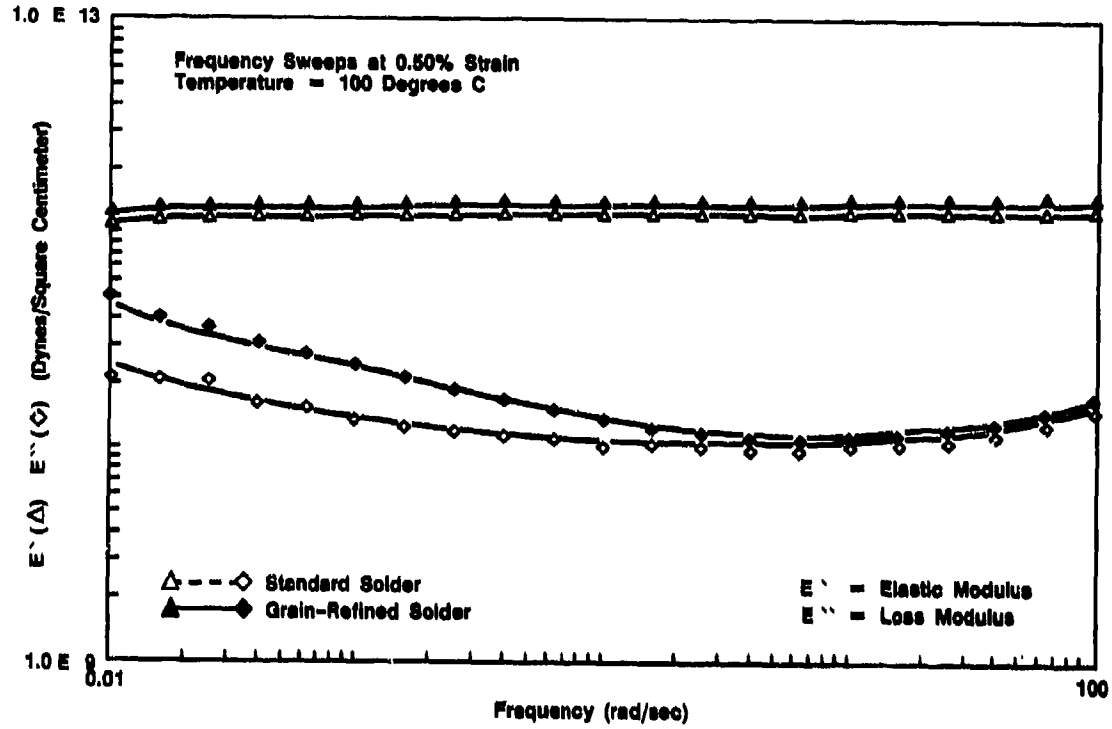

Figure 11. Sn 62 - Pb 36 - Ag 2 solder joint

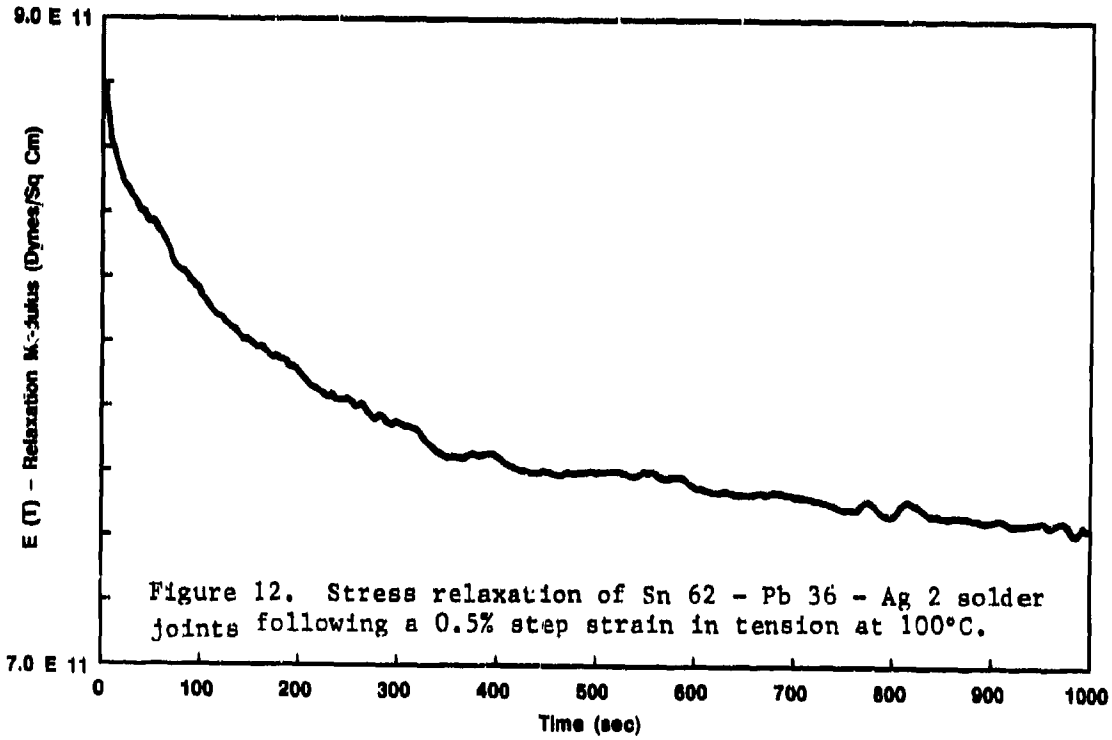

Figure 12. Stress relaxation of Sn 62 - Pb 36 - Ag 2 solder joints following a 0.5% step strain in tension at 100°C.

the extent of relaxation that occurred. This may represent the effect of a compliant resin layer in the printed wiring board substrate to which the solder joints were attached. Such a resin layer could contribute to the observed stress relaxation properties of the solder joint assembly.

The effect of repeated mechanical cycling on the dynamic mechanical properties of solder joints was investigated at -65, 30, and 100 degrees C. Samples were subjected to sinusoidal oscillations with a test frequency of 0.01 radians per second (approximately 10 minutes per cycle) and a test strain of 0.5%. Dynamic mechanical properties were periodically measured during the test.

Initial tests were conducted at 30 dgrees C, with the hopes that the mechanical strain induced by the Rheometrics Dynamic Spectometer would mimic the effects of thermal expansion and contraction of a printed wiring board substrate on a solder joint. Repeated tests, however, failed to reveal a change in dynamic mechanical properties of solder joints as a function of time (or number of cycles). For example, a sample that was prepared from standard Sn62-Pb36-Ag2 solder showed no significant change in either the elastic modulus or the loss modulus after 575 cycles. Upon removal from the RDS, both solder joints were intact. Examination of the solder surface by scanning electronc microscopy showed that, at a magnification of 500X, small cracks could be seen in the solder surface (Figure 13). However, no evidence of cracks in the solder could be seen in a solder joint cross-section that was examined at 100X.

Efforts to conduct time sweeps on solder joints at -65 degrees C were complicated by the fact that the loss modulus of solder at this temperature is too low to be detected. Preliminary tests showed that after 40 cycles at -65 degrees C, no change in the elastic modulus of the solder could be seen. Scanning electronc microscopy examination of the solder surface revealed the presence of numerous small cracks. Microscopic examination of a cross-section of the joint, however, showed that these cracks did not extend into the solder for an appreciable distance.

Major changes in the dynamic mechanical properties of solder joints were seen during time sweeps at 100 degrees C. Figure 14 shows the dynamic mechanical property changes that occurred in a Sn62-Pb36-Ag2 solder joint sample that was subjected to 50 mechanical cycles. The elastic modulus of the solder showed a significant decrease, and the loss modulus showed a significant increase, during the test. In spite of these large dynamic mechanical property changes, both solder joints were intact upon completion of the test. Scanning electron microscopy examination of the solder joint surfaces and cross-sections at magnifications up to 1000X showed no evidence of structural damage to the solder joints.

Figure 13. Scanning electron micrograph of Sn62 - Pb36 - Ag2 solder joint surface after 575 mechanical cycles at 30 degrees C. Test Frequency = 0.01 radians per second; test strain = 0.5%. Magnification = 500X.

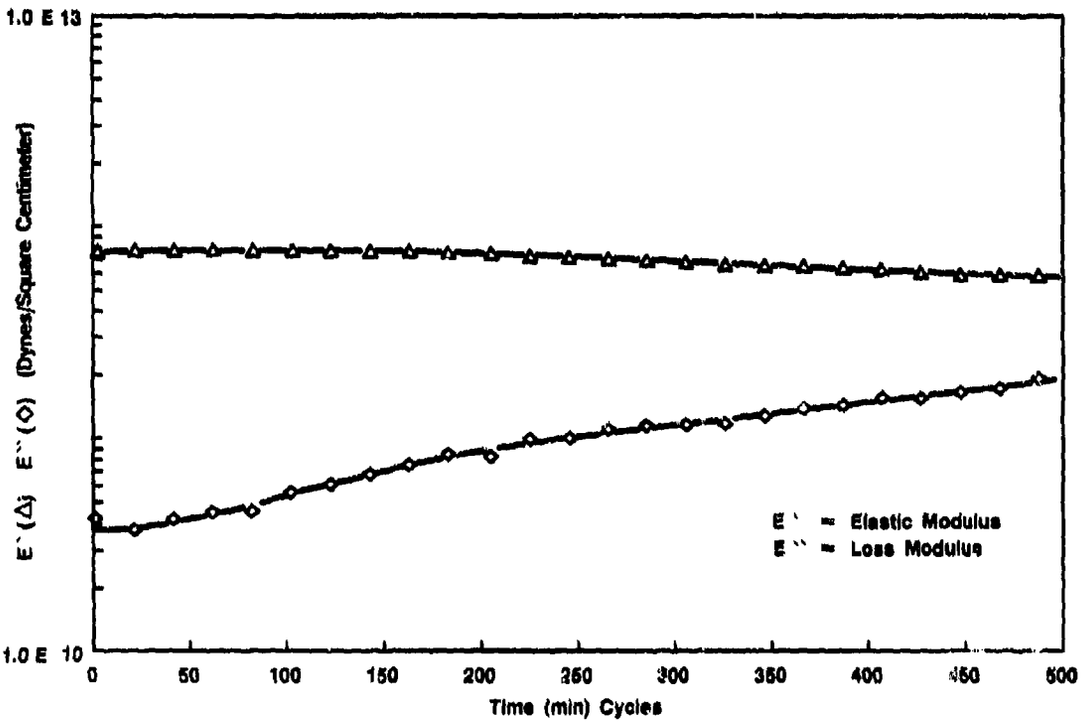

Figure 14. Sn62 - Pb36 - Ag2 solder joint time sweep at 100°c; Test Frequency = 0.01 radians per second; Test strain = 0.5%.

Repeated experiments on Sn62-Pb36-Ag2 solder joints showed the same trend; i.e., at 100 degrees C, repeated mechanical cycling results in a large decrease in the elastic modulus and a significant increase in the loss modulus. However, the rate of increase and decrease of these properties was found to vary somewhat from sample to sample. For example, one solder joint sample reached a point where the elastic modulus was only slightly higher than the loss modulus after only 11 cycles. Mechanical cycling of the sample was stopped at this point, and the solder joints were examined. Both solder joints were found to be intact.

When mechanical cycling was continued beyond the point when the elastic and loss moduli became equal in value, or until the loss modulus had a higher value than the elastic modulus, one or both of the sample solder joints were found to be broken at the conclusion of the test. For example, tests on one Sn62-Pb36-Ag2 solder joint sample showed that the loss modulus and the elastic modulus became equal in value after only nine cycles. After 15 cycles, when the test was stopped, the loss modulus had a higher value than the elastic modulus. This data is shown in Figure 15. Both solder joints in the sample were found to be broken at the conclusion of the test. Examination of the surface of one of the fractured solder joints showed numerous voids that may have contributed to premature failure of the sample (Figure 16). At higher magnifications, the solder surface showed a typical topography associated with fatigue failure (Figure 17). The second solder joint from the sample, while showing fewer voids than the first solder joint, also showed evidence of fatigue failure.

CONCLUSIONS

Based upon the results of work that has been conducted to date, it has been shown that dynamic mechanical analysis is a viable method for investigating the mechanical properties of solder and solder joints under cyclical loading conditions. One major advantage of the test technique is that both the elastic and inelastic responses of solder are simultaneously measured.

Dynamic mechanical analysis has been shown to be sensitive to the well-known strain-rate sensitivity of solder. In addition, the ability of the technique to provide information regarding the stress relaxation properties of solder has been established. The potential ability of the technique to assist in the evaluation of the relative fatigue resistance properties of different solder alloys has been shown not only by the fact that dynamic mechanical test data were consistent with known fatigue resistance characteristics of two different solder alloys, but also by the fact that the technique was successfuly used to predict that two solders that reportedly differed in fatigue resistance would in fact perform almost identically.

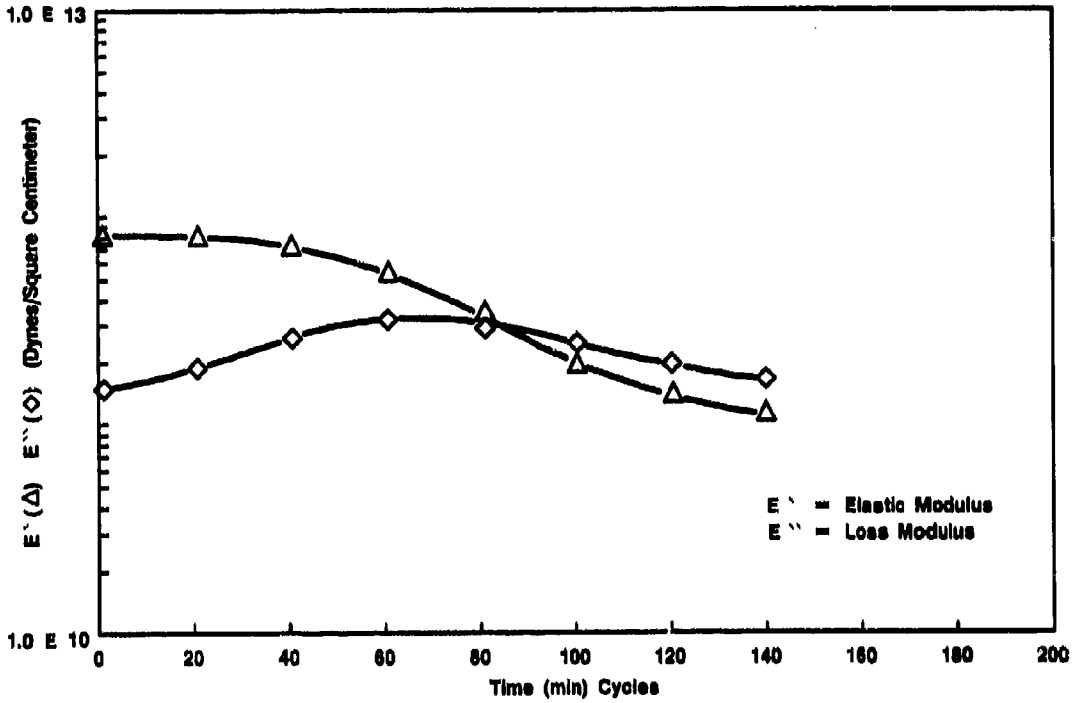

Figure 15. Dynamic mechanical property changes of Sn62 - Pb36 - Ag 2 solder joint sample as a Function of time at 100°C. Test frequency was 0.01 radians per second; test strain was 0.5%. Both solder joints were broken as a result of this test.

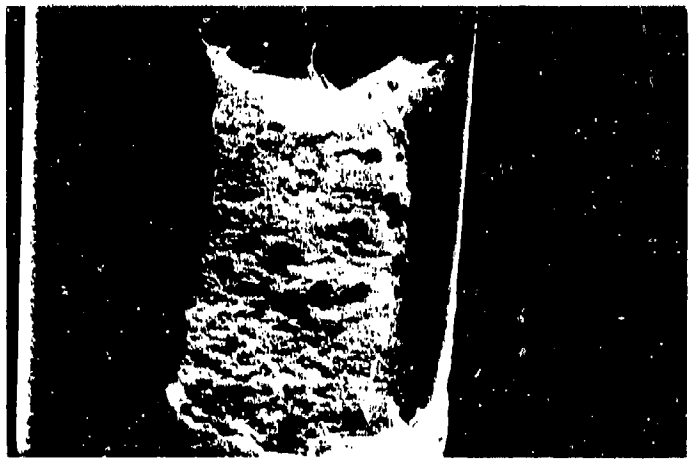

Figure 16. Scanning electron microscope of a Fractured surface of a Sn62 - Pb36 - Ag2 solder joint that broke during mechanical testing. Numerous voids are visible. Magnification = 50X.

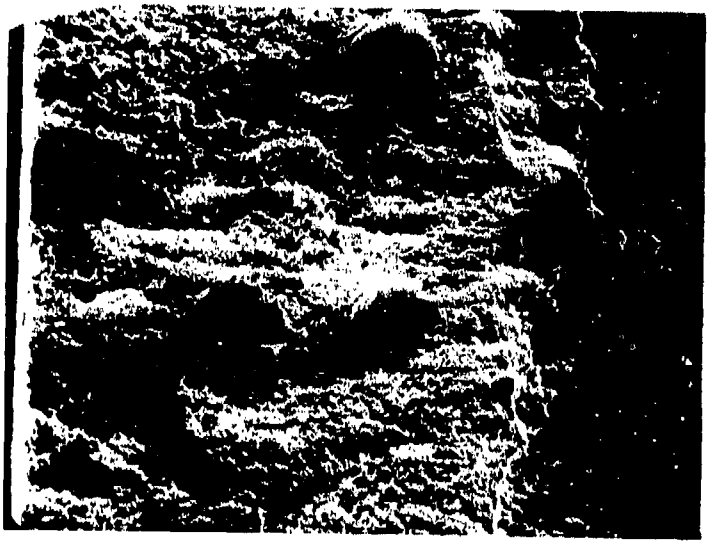

Figure 17. Solder joint surface from Figure 16 at a magnification of 200X.

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STATISTICS, DESIGNED EXPERIMENTS, AND PRINTED WIRING BOARD ASSEMBLY

by
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ABSTRACT

During the past few years, statistical process control and experiment design concepts have taken a prominent place within the industry. The use of such tools within the Motorola, GEG manufacturing environment, has grown to the point where reflow and wave solder process development and optimization has significantly benefited.

The ability to statistically evaluate and model various known and unknown phenomena, has provided GEG's manufacturing technology with a series of very powerful tools to aid in process control and development. The primary purpose of this paper is to present the various approaches used by GEG to implement the previously mentioned statistical tools, with respect to the development of infrared (IR) reflow solder processes and enhancement of certain quality characteristics associated with wave soldered printed wiring boards (PWB's). Beyond specific GEG applications, the paper discuses the role of statistically designed experiments and process control methods as a vehicle for providing answers to complex manufacturing problems. In addition, a discussion of the mathematical and graphical methods underlying the interpretation of quantitative data is presented.

Perhaps the most important benefit derived from the use of statistics to solve manufacturing and quality problems is related to decision making. When experiments are conducted to isolate unwanted sources of process and product variation, decisions must be made to determine whether or not certain experimental effects are important. Through the application of statistics, the researcher can ascertain the mathematical probability associated with the random chance occurrence of various experimental effects. With this knowledge, the researcher can make decisions with known degrees of risk and confidence. Without such knowledge, an organization might possibly expend valuable resources and derive no direct benefit.

Ultimately, the principle reason for applying statistical methods and procedures is to increase quality and yield, while simultaneously reducing costs.

INTRODUCTION

To many individuals the words *statistics* and *probability* evoke a mental image of a mathematician hunched over a calculator or computer, crunching out long lists of meaningless numbers. It is unfortunate that such a mental image exists, as this tends to blind them to the power of statistics used for process control.

From a historical perspective, it is interesting to note that statistics had their origins in gambling. Famous mathematicians such as Pascal, Fermat, and de Mere noted over three hundred years ago that there were distinct mathematical relationships which could help explain the "odds" or chances of winning a given game. (Reference 1) The principles that were formulated to serve the desires of these early mathematicians have been refined to provide a means to model almost any manufacturing process.

Today, process engineers are constantly involved in complex manufacturing environments which have a multitude of hidden factors that can influence product parameters. The work performed in the development of statistics and designed experiment concepts over the past 50 years, has given the process engineer significant tools to develop and control such processes.

The power and importance of Statistical Process Control (SPC) is steadily coming into broader recognition as a philosophy for structuring manufacturing processes. As an example, consider the impact that the concept of "just in time"delivery has had on the quality of products manufactured in Japan. The advantages provided by the "just in time" concept of product delivery have been widely publicized and, as a result, are now beginning to come into vogue within the United States. In order to effectively implement such procedures it is extremely important to have the process under statistical control. If the processes are not under statistical control, then costly bottlenecks can form. It should be noted here, that the root of this concept is a dedicated application of statistics to optimize quality.

The narrative portion of this paper does not center its thrust on the "just in time"concept, rather, it will examine some of the statistical principles that are a part of that concept. As a result, the reader is highly encouraged to extend the concepts and methods presented in this paper to the "just in time" environment. Furthermore, it is not the intent of this paper to provide a mathematical derivation of the statistics presented or the techniques used to develop designed experiments, but rather, a discussion related to the application of the concepts as used at the GEG facility. The bibliography contains a series of works which can serve as a cornerstone to get one started in the field of statistics and experiment design. The examples presented in this paper have been drawn from a wide array of manufacturing processes, ranging from hybrid circuit production to printed wiring board (PWB) assembly.

ORGANIZATIONAL CONSIDERATIONS

The implementation of statistical concepts in a facility will usually involve changing the organizations problem solving culture. This is not a matter that can be initiated without a coordinated plan, supported and communicated from the highest levels of corporate offices. The Motorola Corporation made a significant commitment to establish statistical concepts throughout its engineering staff through a carefully planned and executed effort. To facilitate this task, formal training modules were developed for on site delivery to the general engineering population throughout the corporation. One of the initial objectives of this plan was to create an awareness of the power and utility provided by statistical analysis. Examples provided in the training modules are drawn from widely varying applications collected from the various Motorola facilities. The examples serve as excellent models to show the how, what, and why of a particular concept, and help initiate individuals into the actual "on line"applications. As personnel work with the forming and running experiments on a working production line, two things will happen: a growing confidence of individuals in the statistical experiments credibility and: a realization that there are applications beyond those that exist inside our facilities. The logical extension of these principles, beyond that of a specific in-plant product line, is toward improving the quality of components incoming from suppliers. Thus, it may be seen that the circles of applications for these statistical principles are, in reality, ever expanding.

INTRODUCTORY CONCEPTS

Starting with the fundamentals of central tendency and variability, the statistical base evolves to higher order concepts. One of the concepts likely to be encountered very early in an asserted effort to apply statistics to manufacturing processes, is that of the statistical control chart. Generally speaking, these charts are used to monitor the behavior of a process. Such charts are developed by recording sample measurements taken at discrete periods during production and then plotting the resultant data on a standardized chart. (Reference 2 and 3) In essence, the chart can reveal much information about the basic nature and behavior of the process. In many instances, a statistical process control chart is all that is needed to solve many types of manufacturing and quality related problems.

To better understand the uses of statistical control charts, consider the game of football. As long as the players stay within bounds, the game will be allowed to continue. But when a player steps out of bounds, the game clock stops and adjustments are made to correct the problem. So it is with process problems. The primary purpose of a control chart is to keep the critical process variables within certain bounds so that high quality product may be produced. When the bounds are exceeded, production is interrupted until the source of variation can be isolated and appropriate corrective action taken. Figure 1 displays a typical statistical process control chart.

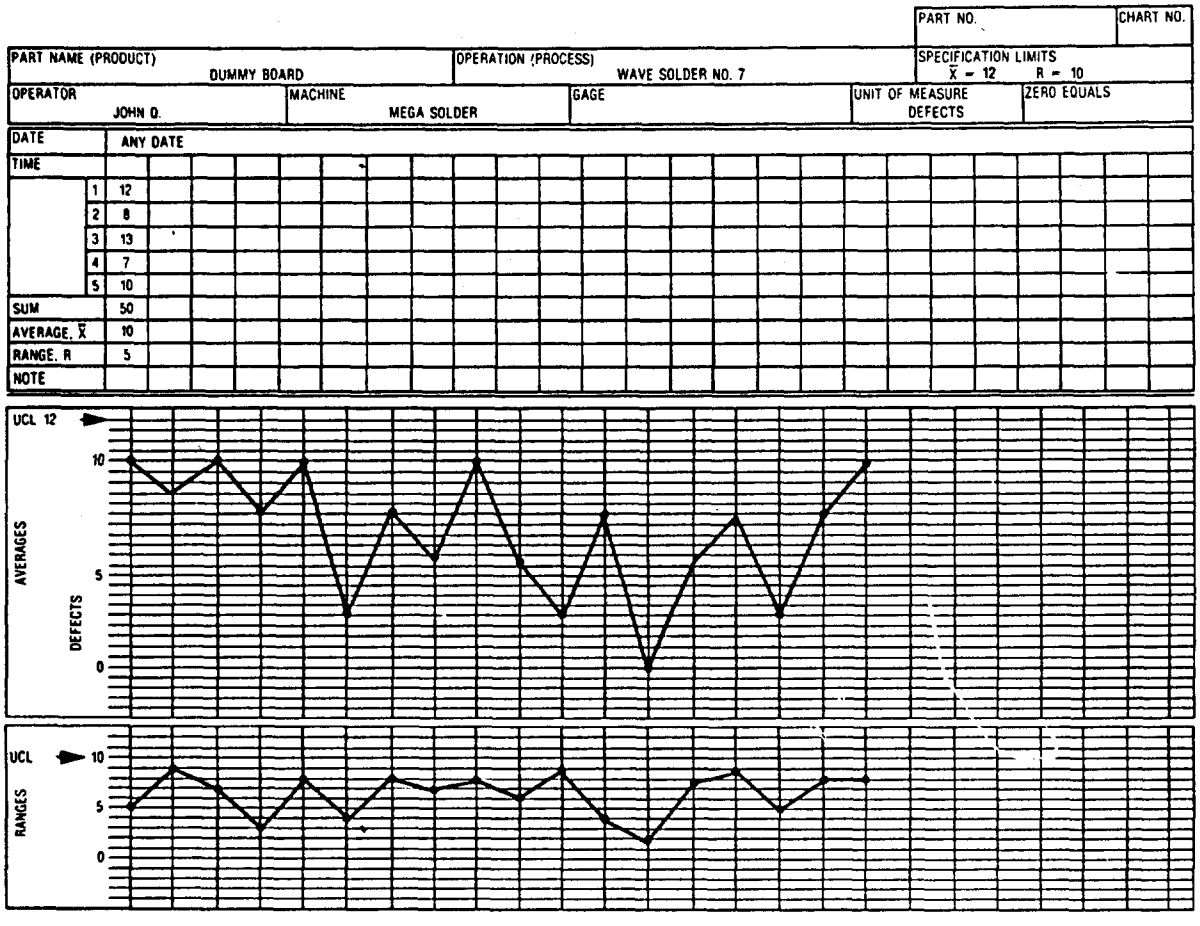

FIGURE 1. Variables Control Chart ($\bar{X}$ and R)

Charts, such as displayed in Figure 1, provide only the mechanism to better understand what is occurring within the process. It is important to realize that the charts do not directly control the process, they only reflect its behavior. It is the function of the process engineer or the operator assigned to the equipment to diagnose and correct out of control conditions. For the chart to be of any real value, the persons involved must understand how to return the process back to the desired control level. If the basic condition which caused the process to run astray is unknown, then a statistically designed experiment can be employed to surface the cause and effect relationship(s).

PROCESS CHARACTERIZATION

Process characterization is central to the derivation of yield and quality improvements. Before a yield enhancement program can be initiated it is necessary to first understand what a particular process is actually capable of producing. Only after characterizing the process in this manner can a reasonable estimate be made of what and how many changes need to occur.

As an example, consider a wave solder process. With this particular application, it may be necessary to run 20 to 40 PWB's to develop the yield characteristics for a given set of material and equipment parameters. Resultant data should be recorded, analyzed, and graphed to provide an understanding of the process behavior and capability. The records generated from this effort can then be used as a frame of reference for future process development work. The following outline presents the basic steps involved with process characterization efforts.
General Step-Wise Progression:

a) Select the operating conditions considered best for wave soldering the PWB's.
b) Run characterization study (20 to 40 PWB's). Inspect and record data.
c) Construct $\bar{X}$ and R charts from the data.
d) Select factors that are suspected of influencing yields, e.g. pre-heat, conveyor speed, flux type, conveyor angle, component preparation, etc.
e) Prepare a full factorial experiment to study effects of varying experimental factors. Run duplicates for each experiment block.
f) Run the experiment after randomizing the experiment sequence. Inspect the PWB's and record the results.
g) Analyze the data after the experiment is finished. This may be done either graphically, by tabulation, or by using statistical analytical programs such as ANOVA. (Reference 4)
h) Evaluate experiment results by running a confirmation test. If the results indicate that a certain configuration of parameters provides the best results, then this configuration should be tested to determine if the results are reproducible. If the results are less than desired, then additional process development is required using Evolutionary Operational Procedures (EVOP). (Reference 5)

EXAMPLES OF PROCESS DEVELOPMENT

Many applications of statistical process development techniques have been employed at Motorola GEG. Such applications range from evaluating PWB's from various suppliers to developing wave solder parameters related to IR reflow soldering. In each of these applications GEG has used process characterization techniques similar to that presented in the step-wise progression.

STATISTICALLY DESIGNED EXPERIMENTS

Let us examine the steps associated with a wave solder process optimization study. The following example illustrates how it is possible to differentiate between the effects of pre-solder processing, wave solder machine parameters, circuit board influences, and solder inspector differences.

In this example a new facility is just starting production with new equipment and PWB's. The first production test runs produced poor inspection yields with abnormally high defects. The primary problem involved determining how to identify the major source(s) of variation which were responsible for the undesirably low solder yields.

To resolve the problem, an experiment was designed. In this particular study three wave solder machine variables, and two PWB in-house processing parameters were evaluated. A full factorial experiment was employed to structure the critical variables for testing purposes. (Reference 6) Each of the variables, was studied at two levels. In this particular case there were 32 different

treatment combinations. Each of the treatment combinations or "experiments"was repeated. This was done to determine the amount of experimental error associated with the tests. The experiment used the following parameters and levels:

Parameters	Levels
Conveyor speed	2.4 and 4.2 feet/minute
Preheat temperature	240 and 277 degrees F.
Solder temperature	500 and 520 degrees F.
Cleaning of board	Clean and noncleaned
Baking of board	Bake and nonbaked

The matrix displayed in Figure 2 illustrates the concept of a full factorial experiment design. It should be noted that the matrix allowed the levels of the variables to be crossed in such a manner as to allow all possible combinations of variables and levels to be explored. Herein lies the power of the full factorial experiment.

CLEAN		CLEAN				NO CLEAN			
BAKE		NO BAKE		BAKE		NO BAKE		BAKE	
SPEED		SPEED fpm				SPEED fpm			
SOLDER	PREHEAT	2.4	4.2	2.4	4.2	2.4	4.2	2.4	4.2
520°F	277°F	702* 711	760 751	762 707	719 714	716 726	753 703	718 759	712 724
	240°F	750 742	708 732	737 741	721 729	755 783	744 739	736 728	746 749
500°F	277°F	725 761	710 743	706 758	705 722	757 747	704 727	748 717	764 733
	240°F	745 736	709 756	701 730	715 734	731 713	740 754	723 720	738 752

* WHERE THE NUMBER IN THE CELLS REPRESENTS THE PANEL SERIAL NUMBER

FIGURE 2. Design of Experiments/Full Factorial

It was determined that 95 percent confidence would be required to justify any changes made to the process on the basis of the experimental findings. Consequently, an alpha risk of 5 percent was selected as the primary decision criteria; i.e., if the outcomes of the experiment stood more than a 5 percent probability of being due to random chance, then the effect under consideration would be classified as statistically insignificant.

The outcomes of the experiment are displayed in Figure 3. This form of tabular data presentation can be used to analyze the data visually for trends or outstanding results. In addition, such a cursory examination requires no mathematical calculations. Often this method will reveal significant information that may be used to direct future investigations. The data has been presented in this format as a means of simplifying the narrative portion of this particular section of the paper. It is anticipated that the reader will recognize the fact that the actual statistical analyses were more than just visual interpretations of the experimental data.

			PWB CLEANED				PWB NOT CLEANED			
			PWB NOT BAKED		PWB BAKED		PWB NOT BAKED		PWB BAKED	
			SPEED FPM		SPEED FPM		SPEED FPM		SPEED FPM	
			2.4	4.2	2.4	4.2	2.4	4.2	2.4	4.2
SOLDER 520°F	PREHEAT	277°F	B - 31* A - 87	A - 141 A - 40	C - 32 C - 23	B - 20 C - 20	A - 36 B - 22	B - 38 A - 56	C - 44 B - 44	C - 20 A - 15
		240°F	B - 105 A - 45	B - 83 A - 62	A - 30 B - 8	C - 54 A - 39	A - 31 A - 44	B - 35 A - 29	B - 18 B - 35	C - 19 A - 35
SOLDER 500°F	PREHEAT	277°F	A - 69 B - 28	B - 222 A - 33	C - 40 C - 36	C - 25 C - 66	A - 15 B - 57	B - 38 A - 23	C - 30 B - 26	C - 14 A - 21
		240°F	B - 24 C - 58	A - 231 A - 66	C - 38 C - 17	C - 86 C - 37	A - 51 A - 13	B - 102 A - 30	C - 22 C - 28	C - 21 C - 47

*WHERE A,B, AND C INDICATE THE INSPECTORS AND THE NUMBER VALUE IS THE TOTAL DEFECTS.

FIGURE 3. PWB Experiment - Defect Summary

ANOVA RESULTS

The analysis of variance procedure (ANOVA) decomposes the total observed variations into component parts, i.e., the total variations due to the main effects and interactions independent of all other effects. In essence, the procedure allows treatment effects to be partitioned from random variations in the data. The comparative statistics are then calculated to provide an observed value which is contrasted against a theoretical value. If the calculated value equals or exceeds the theoretical value, then we know, within certain probability limits, that the effect did not occur by random chance. The data can also be analyzed in such a manner as to provide a percentage which reflects the total contribution of each experimental variable and interaction.

In relation to the previous example, the results of the statistical analysis (utilizing ANOVA) provided insight into the synergistic effects of solder equipment, setup parameters, and presoldering processing operations. The analysis of variance procedure was executed via SPSS-X (C) software.

An interpretation of the computer output indicated that the effects of precleaning/no precleaning and baking/no baking prior to insertion and wave soldering were statistically significant. The remaining effects failed to reach or exceed the decision criterion; therefore, the associated factors were considered statistically insignificant. The results from the analysis are presented in percentage form and listed in Table 1.

Not all the results reported above are significant at the alpha 0.05 level. Some required increasing the level to 0.10 before a statistically significant value could be achieved. At the alpha level of 0.05 only the effects of baking/no baking and cleaning/no cleaning are significant. This suggests that only 23.1 percent of the solder defects can be attributable to the presolder conditioning. If the alpha risk is increased to 0.10 then conveyer speed and the baking/cleaning interaction become significant, this would add 10.1 percent to the explained defects. The 60.8 percent residual provides a rich source to look for variations within the PWB's themselves. These results are displayed in Figure 4 in a standard Pareto format. Thus, the influences over the levels studied, of the wave solder machine parameters, presolder conditioning, circuit board material influences, and inspector bias have been evaluated and all these effects have been accounted for.

TABLE 1. Results from ANOVA Analysis

Effect Analyzed	Percent Variation in Solder Yields
Baking/no baking	12.9%
Cleaning/no cleaning	10.2%
Conveyor speed	5.1%
Solder temperature	1.7%
Board preheat temperature	0.2%
Interaction between baking and cleaning	5.0%
Interaction between conveyor speed and cleaning	4.1%
Inspectors	0.5%
All other effects	60.8%

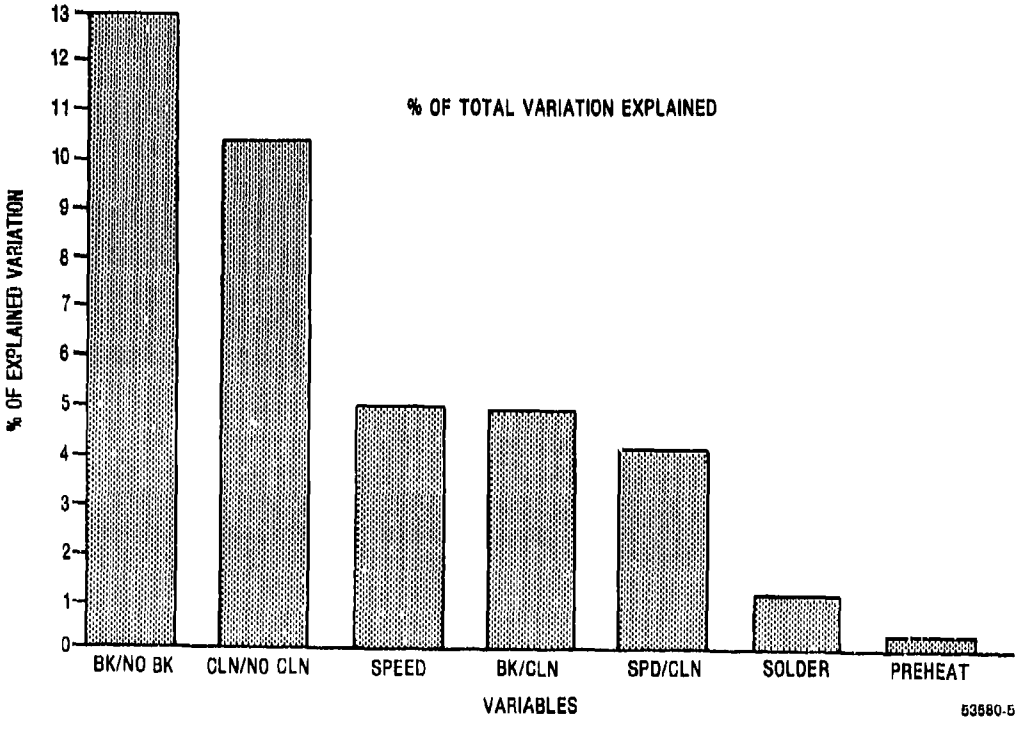

FIGURE 4. PWB Solder Analysis

GRAPHICAL INTERPRETATION OF RESULTS

The results from designed experiments can be examined graphically to aid in the understanding of the effects of the experimental factors. (Reference 7) The principle advantage of graphical analysis techniques is that the graphs allow a visual presentation of the effects of various combinations of factors and levels. Sometimes the graphical methods offer a much clearer understanding of these combined effects than just pure numbers can provide. The graphical presentation is limited to three dimensions at a time, therefore the four factor and above graphical presentations of simultaneous interactions are not possible. However, the graphical analysis is a very fast tool to determine interactions and provide an overall sense of output property direction. Examples of graphical presentations are show in several applications in this paper. Two level one factor, two level two factor, and three level two factor analysis are shown later in this presentation. Each of these graphic forms provides a different source of information. As an example of a two level one factor analysis, Figure 5 provides the data to assess the effects of a single factor main effect at two levels. The example in Figure 5 is a very simple plot of the dependent variable, which is the total number of defects obtained from the independent variable of two different conveyor speeds across a wave solder machine.

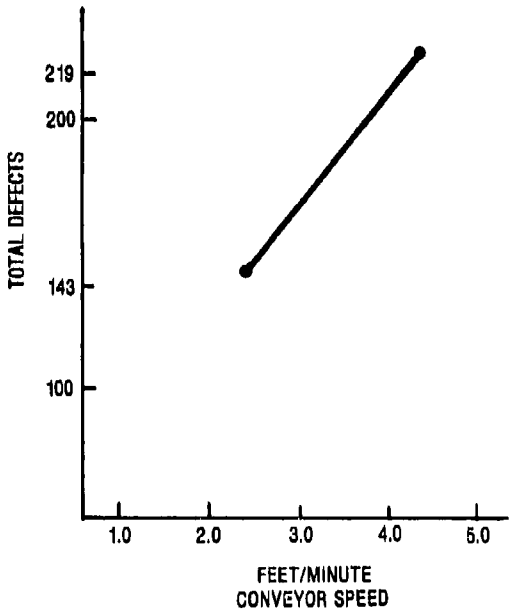

FIGURE 5. Main Effects of Conveyor Speed

FRACTIONAL FACTORIAL EXPERIMENTS

Fractional factorial experiments are another useful concept found in the statistical tool bag. (Reference 8) Somewhat like a full factorial in its original structure in setting up the factors and levels, the fractional factorial experiment differs in the number of experiments required and the amount of data captured. The fractional factorial experiment has an advantage when used in a screening application, and is a very useful concept when faced with a large experiment matrix,

such as a seven factor at three levels. This type of experiment would result in a full factorial of 2187 different experiments, which is a rather large undertaking in any facility. But the same experiment could be screened with 81 experiments or less to determine if the combinations selected were providing results close to those desired. From this it can be seen that when faced with a large range of factors and levels to evaluate, the fractional factorial experiment will save time, money, and resources, and still provide a good screening of those factors. The fractional factorial experiment is developed from a specific sampling format taken from the full factorial format. The pattern generated from the levels and factors provides a statistically valid sampling plan that can be analyzed using, among others, ANOVA techniques. One of the areas of complication that tends to arise in fractional factorial experiments is the aspect of interaction beyond the main effects. That is, what are the contributions to the total level of effects that are attributable to the second and third order interactions? These interaction effects are difficult to calculate above the third order interaction, and because of this, the higher order effects usually do not provide significant influences and therefore are considered to be negligible.

As an example of the use of a fractional factorial experiment, let us examine the following experiment run to minimize solder defects through optimizing wave solder machine parameters. This experiment utilizes results obtained from previous work run to determine the main factors effecting yields from the wave solder equipment. It is from this preliminary work that the factors and levels for this study were derived. This experiment examines six factors. Five factors examined at two levels, and one factor examined at three levels. These factors all relate to the wave solder equipment operating parameters. The experiment matrix is shown in Figure 6.

					SOLDER TEMPERATURE							
					475°F				510°F			
					FLUX DENSITY				FLUX DENSITY			
					0.886		0.906		0.886		0.906	
					SPEED FPM		SPEED FPM		SPEED FPM		SPEED FPM	
					2.2	5.0	2.2	5.0	2.2	5.0	2.2	5.0
PREHEAT SETTING	250°F	OIL LEVEL LOW MEDIUM	WAVE HEIGHT %	100	34*			186	52			58
				50		131				96		
				100		90				38		
				50								
	200°F	OIL LEVEL LOW MEDIUM	WAVE HEIGHT %	100		132	57			190	44	
				50	32			141	38			88
				100	27			174	128			72
				50		73	33			52	23	
	NONE	OIL LEVEL LOW MEDIUM	WAVE HEIGHT %	100								
				50			56				95	
				100			128				41	
				50	98			186	85			88

* PWB PANEL SERIAL NUMBER

FIGURE 6. Fractional Factorial Experiment
Wave Solder Experimentation Parameter Settings

Process interactions are shown graphically in Figures 7 through 9. These graphs are plotted from data obtained by measuring the dependent variable output data, in this case total defects, resulting from operation of the wave solder machine at each of the two factor levels shown. Two factors are plotted together on one graph to show the effects that occur when these factors are operating together at various specified levels. The interactions between two factors is evidenced by the nonparallel position of the lines of each graph. Interactions are graphically observed where the data plotted produces a graph with crossed lines, indicating a reversal or increase from one factor combination to the other.

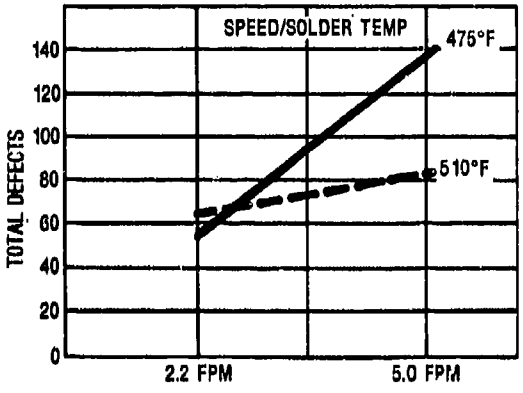

FIGURE 7. Conveyor Speed

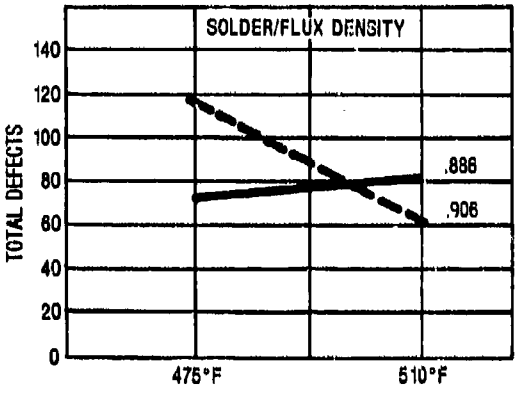

FIGURE 8. Solder Temperature

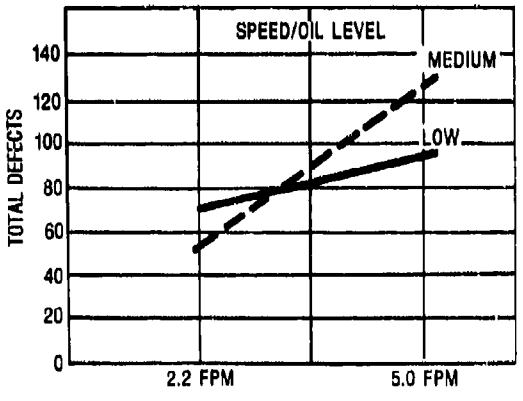

FIGURE 9. Conveyor Speed

PROCESS CAPABILITIES PREDICTION

An application used at Motorola, GEG, involved monitoring the gold plating on PWB's to achieve a wire bond of consistent quality. The circuit utilized an assembly technique where several integrated circuits (IC's) were used as a part of the circuit assembly. The initial problem was one of developing consistent wire bond pull strengths with acceptable standard deviations. The circuit board manufacturer had set up a gold plating process specifically to supply wire bondable, gold plated PWB's for this design. The supplier's previous gold plating experience had been in plating edge contacts on PWB's with hard gold, which is a totally different requirement than that of a wire bondable gold.

To solve this problem, and to help reduce the product rejects at incoming inspection, Motorola worked with the supplier to develop a process characterization of the plating process as it related to the wire bondability of the resultant plating. Samples were plated and wire bonded. These were then subjected to wire pull testing, and the data was evaluated to determine the projected process capability. A computer program was generated to analyze the results of the wire pull tests. Wire pull data was entered into the computer and the resultant statistical information printed out the projected wire bond limits that could be expected from the circuits in that lot, based on a 95 percent confidence limit. This printout also provided an accessment with a known probability of what percent of the product that would fall below the lower acceptance limit, should there be any in that category. Figure 10 is a graphical presentation of the range of wire bond pull strength values derived from a normal distribution, based on the information obtained in lot sample testing. In this particular case there is a 95 percent probability that 1.1 percent of the product will be below the 2.0 - gram limit, therefore rejecting the test lot. Figure 11 is a close-up of the tail of the lower limit of the distribution as shown in Figure 10.

The examples shown in Figures 10 and 11 were very instrumental in measuring the overall improvements in the development of the plating processes. These concepts are not new, they simply illustrate the power and information that is resident in statistical procedures that already exist. Statistical calculations may provide meaningful data from even the simplest of formulas.

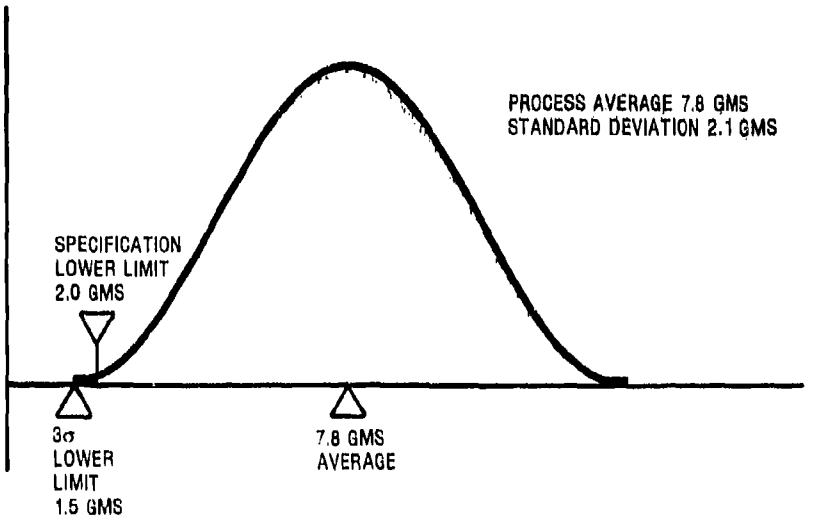

FIGURE 10. Distribution of Wire Pull Strengths

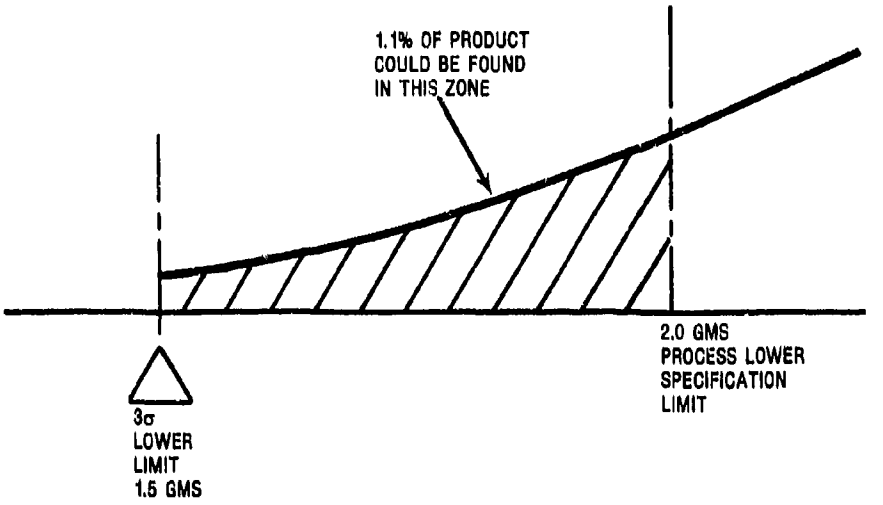

FIGURE 11. Detail of Lower Limit Tail

Another example of the use of comparative statistics is the application where one wishes to determine if there are significant differences between groups of data. Let us consider a wave solder line that has been producing yields that appear to be quite variable. There is an unfounded suspicion that the variation in wave solder quality is caused by wave solder machine set up parameters varying during the production run. This is a good example of how raw results can be quite deceiving, for as we shall see, it takes more than a casual examination to obtain the facts. Upon looking into this problem, mixed lot date codes were found on the PWB's used in the wave solder production runs. The lot to lot variation in the PWB's indicated a potential for a significant contribution to this variation in wave solder yields. To check this hypothesis, a series of wave solder tests was run on sample PWB's selected from one supplier's lot of date code boards. If the wave solder equipment was randomly varying from its operational parameters, then these effects should be found in the solder quality of boards from a known "good"lot. The experiment was set up to evaluate wave solder machine operating parameters on three different days during a weeks production operation. These three days would also be separated from one another by at least one days production. This allowed the worse case conditions to occur, in that it also included an equipment tear down and set up. 16 PWB's were scheduled for this experiment; six used for the first day, four for the second, and six for the third day. All the PWB's were run using a given set of operating parameters. With the daily changes in set-up that happen as a normal occurrence, there would be ample opportunity for the effects of nonreproducibility of equipment set-up to occur if it indeed was the significant contributing factor to the solder yield variations. To counteract time related effects, all the circuit boards were run within a specific time period each time. The boards were inspected by the same inspector after cleaning, and the defects were recorded. After all three groups were inspected the results were examined. At first glance it appeared as though there was a significant difference in the results, for one days group "clearly looked better"than the others. But upon statistically examining the results with a Student t analysis, it was shown that there was no statistically significant difference between the three groups of data. (Reference 9) The results of this experiment are shown in Table 3. The analysis of the results from

this experiment indicated that the equipment was not the single source of the problem of varying yields, and that the production groups with the mixed lot date codes should be examined to determine their effect on yields.

TABLE 3. Results From Solder Inspection

	Group 1	Group 2	Group 3
Sample size -- PWB's	6	4	6
Insufficient solder	2	0	0
Excess solder	2	6	9
Poor Wetting	27	13	15
Blowholes/depressions	37	16	26
Shorts	5	0	1

RANDOMLY SELECTED TEST COMBINATIONS

This experimental design method was used to examine the effects of inert gas flow rates in a six zone IR reflow furnace. The effects of gas flow on the zone temperatures was an unknown factor in setting up the IR reflow equipment. To resolve this question an experiment utilizing a randomly selected test combination technique was initiated. (Reference 10) This experiment design is a screening tool used in cases where there is a large number of factors and levels in an experiment matrix. This test method generates the experiment matrix from a balanced combination of test factors. The resulting total number of experiments is usually less than a fractional factorial, although this is not a fixed rule. Normally, the sample size is 1 to 5 percent of the size that would result from the full factorial experiment. This experiment design has an inherent disadvantage in that the confidence levels cannot be established in estimating the effects of factors. This is due to the fact that the data generated from the experiment can only be analyzed graphically for trends. The main effects produced in the experiment are observed as the steepest slope plotted. The effects of the most significant factor(s) can be removed mathematically to reveal the next most significant factor. This may continue until all the significant factors have been tagged. This process can very quickly provide information that will allow a more appropriate selection of factors and levels to be run in a follow on experiment, thus enhancing an optimized result.

In the case of the IR reflow experiment there were eight factors at three levels that would result in 6561 experiments in a full factorial format. This experiment used only 99 samples to screen all factors. The results from this experiment are being evaluated at this time. The initial findings appear to suggest that the inert gas flow rate is not a significant factor and the reflow zone temperatures are not effected by varying flow rates. The most significant factor appears to be conveyor speed.

Figure 12 is shown as a demonstration of the graphics analysis to show the interrelationships of independent factors. The independent variables shown on the X and Z axis in this example are the inert gas flows into the reflow zones and conveyor speed. The dependent variable in the Y axis is the resultant temperature in the reflow zones. This graph shows a two factor three level result of the effects of inert gas flowing through the reflow zones of an IR reflow machine.

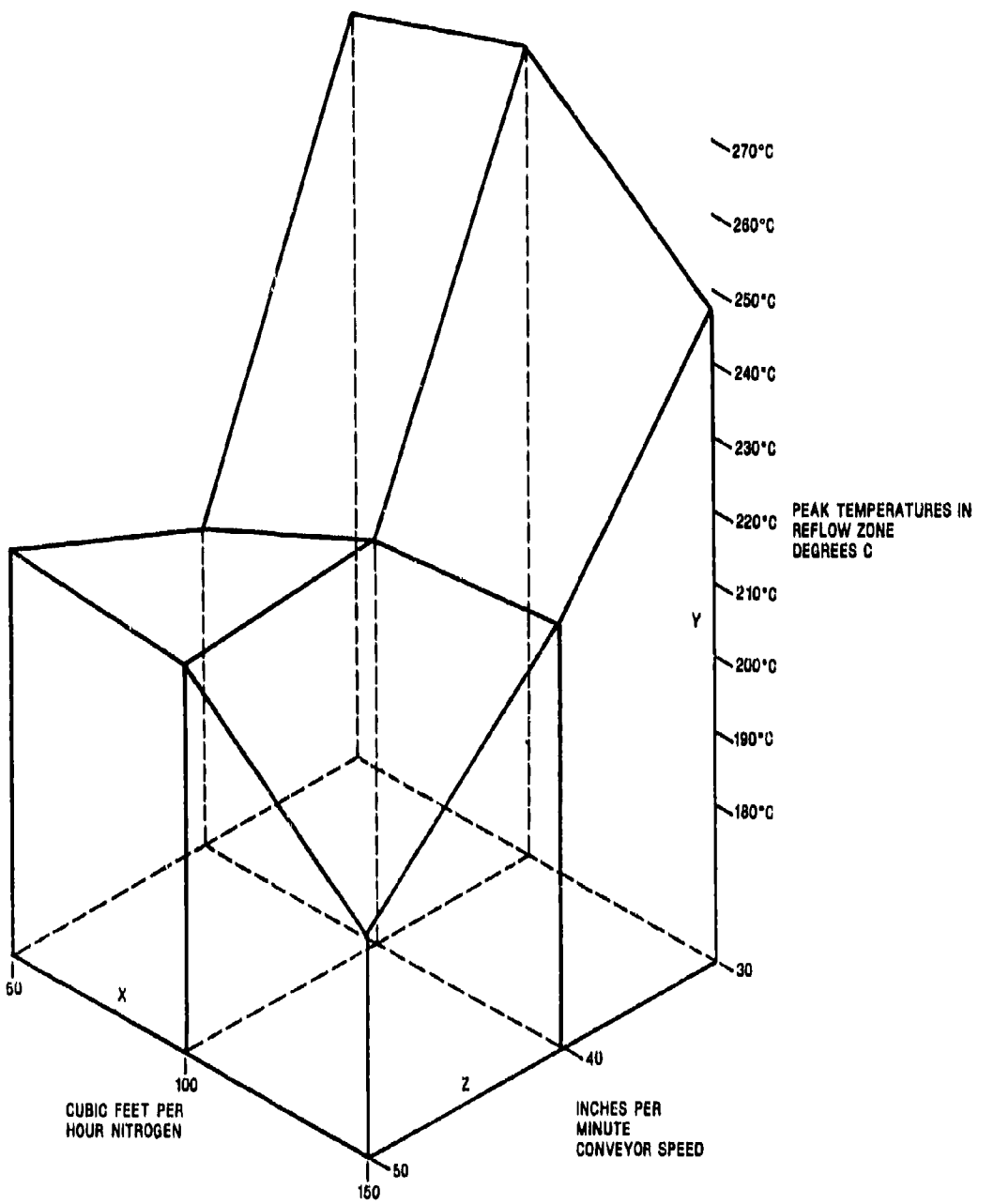

FIGURE 12. Three Dimension Graph

CONCLUSIONS

The applications presented in this paper represent only a few of the experiments that have been run at Motorola, GEG. The results obtained from these experiments have provided valuable insights into many complex problems.

The statistical methods presented in this paper have greatly benefited Motorola's understanding of the complexities of inter- related factors effecting PWB wave soldering. Prior to the implementation of statistical analytical methods the combined effects of materials, pre-process conditionings, and process induced interactions, created a confusing array of possible solutions, and required considerable time and resources to find an appropriate solution. Through the use of these analytical and statistical principles, complex problems can now be resolved in a timely manner with moderate usage of resources. Wave solder process characteristics can now be formally documented to provide a meaningful assessment of process changes.

The techniques presented in this paper are not intended to represent the only analysis methods that may be used, rather they are only a small sampling presented to show the application variety. There are many other methods that may be used to provide answers to process related questions. The examples shown in this presentation have been some what limited to PWB applications and wave solder evaluations. However, this does not mean that these are the only applications for these principles. The statistical design concepts and analytical techniques presented here could be used to make significant contributions in design engineering applications with reduced development time, potentially lower overall development cost, and optimized designs as an output of their use.

The concepts of statistical process control continue to be pressed into more extensive application as the training spreads throughout the GEG facility. These techniques will ultimately become the order of the day, rather than the exception, for the daily operation of all Motorola, GEG, Tactical Electronics Division (TED) projects.

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REAL TIME AUTOMATED INSPECTION OF SMD SOLDER JOINTS

by

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ABSTRACT

The historic dilema of Process and Quality Control lies in the balance between yield loss and customer rejections vs time, consumables, and extra personnel required for testing. How much time can be gained from a given investment in additional equipment and operating expenses?

The new process control tool, micro-focus real-time radiography, addresses all of the traditional drawbacks of testing while providing more information. Testing is accomplished, non-destructively, with no sample preparation, on the production floor with production personnel.

Thus, process deviations are detected, quantified, and appropriate adjustments are made or unsalvageable problems are rejected early in the process. Applications span all aspects of the electronic industry; semi-conductor, hybrid circuit, discrete component, multi-layer PCB and surface mount technology. The ability to see high atomic numbered structures as small as .001" encapsulated in lower density materials are preferred applications. Nicolet Instruments Mikrox system addresses these inspection needs.

THE X-RAY PROCESS

A mixture of technology is required to develop real-time x-ray imaging. The Nicolet Mikrox system has the ability to magnify from 20 to 50 times like a microscope and peer inside objects like and x-ray machine. The X-ray tube operation consists of electrons being boiled off the filament of the cathode and striking a tungsten target on the anode, thereby creating x-radiation. The penetrating power of the x-rays is determined by the kilovoltage applied to the potential difference between the anode and cathode.

To complete the x-ray process at least a portion of the radiation must pass through a sample in order to create an image on film or on an x-ray sensitive camera (used for real-

time viewing). More radiation will pass through a void (flaw) or lack of material and will show as a lighter area on a video display. Areas that are more dense and absorb more radiation will appear darker.

The unique resolution characteristics of Mikrox are partially attributed to the finite size of the focal point from which the x-rays are generated. This focal spot measures approximately 10 microns.

SMT INSPECTION REQUIREMENTS

The ability to establish and monitor SMT process parameters is absolutely retarded without the ability to visualize the condition of the solder connections beneath the surface-mounted component. Five specific problems which are most common during the surface mount process can be detected with x-ray imaging.

- Solder Balls
- Solder Bridging
- Solder Voids
- Lack of Solder & Poor Fillet
- Component Misregistration

REAL-TIME X-RAY APPLICATIONS

Generally four levels of inspection are addressed through x-ray imaging.

- Failure analysis for laboratory use in establishing quality parameters and monitoring at a research an development level. Rotational capabilities allow for multiple viewing angles of the specimen.

- Medium production level and on-line process control. A manually controlled system with x-y movement and large area of view for monitoring all levels during the manufacturing process.

- Automated with x-y programmability. A system requiring operator judgement can be networked with other intelligent equipment such as rework and repair situations and drill equipment.

- Automatic with image recognition. Computer aided decision making is integrated to the automatic system with x-y programmability.

AUTOMATED INSPECTION

There are many reasons for needing an automated system, (high volume, 100% inspection, programmability, repeatability, networking), but it all boils down to one issue: the need for an effective, accurate means of controlling the manufacturing process.

An automated system with the above features can accomplish this task, but still requires human judgement.

Through the integration of automatic image recognition, the on-line operator requirement is eliminated. By taking the electrical output of the x-ray sensitive camera, a computer evaluation can be made.

Driven by a 68010 microprocessor, the vision system can inspect approximately 1" square of populated every 4 seconds. Problems detected are quantified, x-y position is defined and the reporting cycle is completed through hard copy printouts, or electronic storage of the data. Thus, an automated system provides continuous, closed loop feedback to pre and post manufacturing processes.

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CIRCUIT CARD ASSEMBLY INSPECTION OF SURFACE MOUNT COMPONENTS UTILIZING A MACHINE VISION CONTROLLER

by

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January 5, 1986

ABSTRACT

This paper describes the benefits and operation of a machine vision controller for surface mount technology process control. The paper outlines economic benefits with an example of savings realized by machine vision detection of defective assemblies before they reach the field. A description of the vision controller's function at each step of the assembly process shows how feedback to process control provides short process correction time, reduction in repair and labor costs, increased yield and improved quality control.

INTRODUCTION

As more and more manufacturers begin to utilize surface mount technology (SMT), the need for process control of the automated system becomes apparent.

To realize the benefits of SMT, the manufacturer must ensure that the automated manufacturing system will yield quality products the first time at production-line rates (sometimes exceeding 100,000 circuit boards a week). This reasoning becomes apparent when one investigates the following:

- Market studies indicate that it will cost $25 to repair a typical circuit board if the repair is made in the automated process.

- If the defect is not detected and repaired until the circuit board is placed into the system, the cost to repair it is typically $45. If the defect is not detected and repaired until the system is placed in the field, the cost to repair it is typically $220. In more advanced applications (such as in military or aerospace), the cost may range in the millions.

Defects that are recognized in the field are those that have not been detected by conventional in-circuit or in-system tests. These defects tend to be those that result from marginal tolerances that can only be detected by visually inspecting the components.

If one is producing 100,000 circuit boards a week, the following cost impacts are interesting:

- If one assumes a 90% first-time yield of a good board; then 10,000 boards have to be repaired at a cost of $250,000 a week.

- If one assumes that 99.9% of boards that pass electrical test are good, one then ends up with 100 bad boards or a cost of $4,500 per week or $234,000 a year.

- If one assumes that 99.99% of boards that pass system test are good, one then ends up with 10 bad boards or a cost of $2,200 per week or $114,400 per year.

From this analysis, it becomes apparent that the most important aspect of manufacturing the product is to ensure maximum first-time yields and to minimize the high cost associated with repairing the circuit board later.

Utilization of machine vision controllers in the process will ensure a major decrease in production and repair costs by:

- Dramatically improving first-time yields
- Dramatically reducing the overall defects not detected by electrical testing

SYSTEM OVERVIEW

FIGURES 1 and 2 outline the typical SMT manufacturing process and associated process control issues.

The overall system utilizes a host computer and a series of distributed machine vision controllers (MVC) that incorporate an Image Flow Computer, personal computer, camera positioner, and man/machine interface. The MVC is used to monitor and control each major subsystem in the overall process. These subsystems typically are:

- Solder Paste Deposition
- Component Placement (sometimes multiple)
- Solder Reflow

HOST SYSTEM

The host system monitors and controls the overall performance of the system.

The host performs the initial line setup whereby the circuit board set-points are sent to the MVC. Such set-points would include:

- Solder Paste Amount and Location
- Component Types and Locations
- Final Solder Amounts
- Final Component Locations
- Set-Point Alarm Tolerances
- Alarm Limits

SMD Board Coordinate System

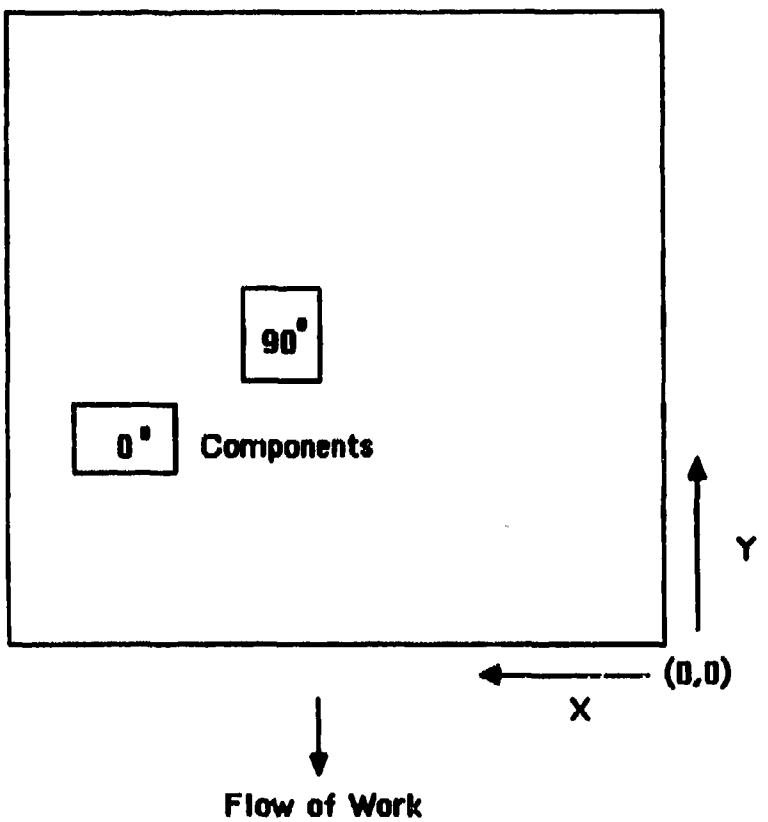
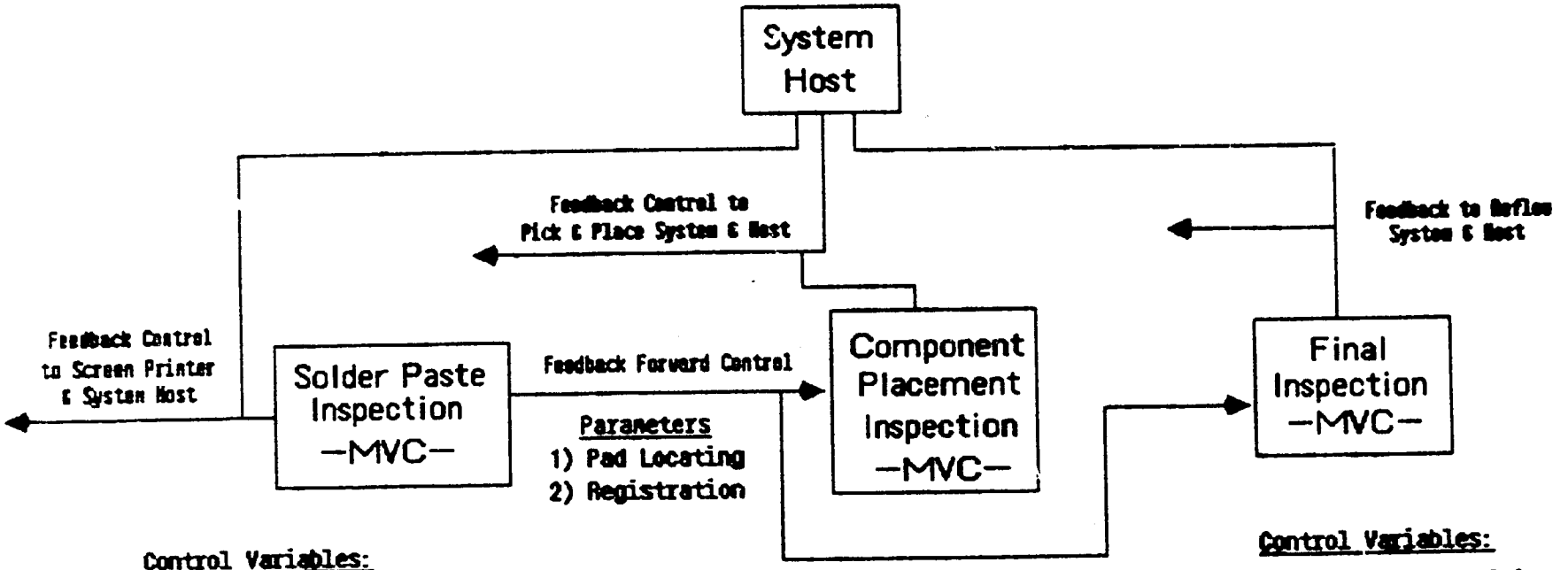


FIGURE 1

SMT System Process Control Overview



Control Variables:

1) Screen Alignment
2) Amount of Solder
3) Position of Solder

Control Variables:

1) Component Absence/Presence
2) Component Position (x,Y,Theta)
3) Lead Position on Pad for 50 mil Spacing or Less
4) Polarity
5) Correct Part
6) Coplanarity of Large Active Components

Control Variables:

1) Final Component Position
2) Absence/Presence of Solder
3) Bridging
4) Voids
5) Shape

FIGURE 2

The host would also monitor trends in the process so dynamic corrections may be made to the process if system variables are reaching alarm limits. In extreme cases, the host may decide to shut down individual pieces of equipment if they exceed critical tolerances. Such an example may be an in-line process where there is no human involvement.

SOLDER PASTE DEPOSITION

The MVC would inspect the circuit board to ensure:

- That pattern registration is within specification, precisely measuring offsets to reference locations so pads can be located for later use in the process.

- That the solder paste is located properly and is the right amount.

If deviations are noted from set-point tolerances, corrective action can be taken by the host or the screen printer.

If board registration is out of specification, the board would be diverted out of the process.

COMPONENT PLACEMENT

The MVC will be utilized to inspect each circuit board to ensure that all components are correct and are located properly.

In the case of chip capacitors, chip resistors or active devices that are placed by high-speed pick and place units (3-6 parts per second) the MVC will inspect to tolerances of 3-10 mils to ensure that the component is positioned properly on the pad.

The MVC utilizes high-speed morphological grayscale operations to ensure that the leads are covering a given percentage of the pad. It should be noted that the system will have an accurate position for each pad as fed forward from the initial MVC. Likewise, it can be assumed that the solder paste is positioned properly and that the position of the solder paste is known relative to the pad.

If a component is positioned improperly on the pad, the precise location of the centroid of the component can be measured utilizing a high-speed "connected component" algorithm. This positional data can then be fed back to the pick and place unit and to the system host.

For active components (usually 50 mil lead spacing or less) placed by robots (1-2 parts per second) or other pick and place units, the MVC will do a high-resolution inspection (1 mil tolerance) to ensure that individual leads are precisely located on pads.

For components with leads that have very fine spacing (25 - 40 mils), it would be recommended that the leads be inspected for coplanarity and spacing before being placed.

The location of the pads and solder paste is fed forward from the initial MVC such that the inspection task becomes that of locating the individual leads to a given board (system) reference. If the device has been inspected for coplanarity and spacing before placement, the system will not be required to inspect all of the leads on a given device.

It is also noted that a more detailed inspection of these active devices is necessary to ensure that part numbers and polarities are correct.

If system tolerances are violated, then corrective action can be taken.

FINAL INSPECTION

The MVC will be utilized to ensure that components did not shift during the reflow process and violate given set-points.

The system will inspect individual pad locations to ensure that the proper amount of solder is present and that there is no excessive bridging between pads.

As before, the individual pad locations are known and can be used in this analysis.

The MVC also can be integrated with an X-ray unit to provide grayscale images of individual solder joints in order to do a detailed inspection of individual solder joint for:

- Shape
- De Wetting
- Internal Voids

LEAD-THRU-THE-HOLE INSPECTION

Many manufacturing processes will incorporate "lead-thru-the-hole" (LTH) technologies with the SMT process.

In such processes, the SMT devices will be mounted on the same side of the board as the leads before wave soldering.

In this process, the MVC would also inspect the leads for:

- Absence or Presence
- Length
- Clinch Angle

REPAIR LOOPS

Individual repair loops can be provided at each subsystem so defective boards can be isolated and repaired quickly.

Quick identification of errors can be done by directing a light beam to the defect or by providing a graphical output to the repair person indicating the location of the defect.

Component misplacement or absence will be accomplished utilizing robotics with feedback from the MVC.

JUSTIFICATION

If one assumes that this process control system improves the first time yield to 95%, the weekly cost is reduced $125,000, notwithstanding the other cost benefits associated with:

- Faster Correction Time in Process
- Reduction in Repair Costs
- Reduction in Labor Costs

The operators safety would also be improved because they would be removed from the manufacturing process.

Mike Buffa attended West Point and received a BSEE degree from West Virginia University in 1968. During his 10-year career with General Electric and Honeywell, he worked in the field of industrial automation. His activities included control system design programming, project management, and management of a technical support group for the Honeywell Corp. in Europe. His engineering experience involved the automation of refineries, steel mills, nuclear power plants, pulp and paper mills, and chemical plants. As Vice President of the Electronics Systems Division for Machine Vision International, he is pioneering machine vision technology for various applications in the electronics industry.

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NAVY SOLDERING TECHNOLOGY TRAINING PROGRAM

by

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ABSTRACT

Many changes have taken place recently and are continuing to take place in the field of electronic assembly and production. Key changes affecting manufacturers of Government hardware include the issuing of new and revised Standards and Specifications pertaining to electronic assembly, fabrication and soldering processes. The new Standards and Specifications necessitate revisions within the Soldering Technology Training Program to incorporate the changes. This presentation will provide a status report on current and planned revisions to the training program. A detailed discussion of new training courses, new certification levels and additional training sites will be provided. Implementation plans and schedule for the field recertification of instructor/examiner personnel will also be covered in detail.

TRAINING PROGRAM STATUS OUTLINE

NAVAL WEAPONS CENTER ROLE

SOLDERING TECHNOLOGY ORGANIZATION

SOLDERING TECHNOLOGY TRAINING

TRAINING COURSES

Courses Offered

Course Revisions

New Courses

CERTIFICATION/RECERTIFICATION

New Certification Levels

Operator/Inspector Recertification

Field Recertification Implementation

TRAINING PLAN REVIEWS

NEW/REVISED SPECIFICATIONS

NAVMAT Instruction 4855.10

WS-6536 Revision "E"

DOD-STD-2000

NEW TRAINING SCHOOLS

William E. (Bill) Sake, NWC's own Director of Soldering Technology Training, has 25 years experience in electronics, with 16 years in education and product assurance for electronic assembly and soldering processes. Bill developed and authored the training and certification program used by all naval aviation military activities for electronic assembly soldering and repair processes.

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